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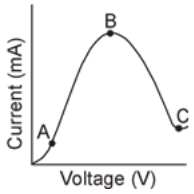
Q1. The graph shown in the figure represents a plot of current versus voltage for a given semiconductor. Identify the region, if any, over which the semiconductor has a negative resistance.



Q2. What is acceptor impurity?

Q3. What is the value of forbidden gap energy of silicon and germanium?

Q4. Why semiconductors behave as insulators at 0 K?

Q5. Why the crystalline substances have a sharp melting point?

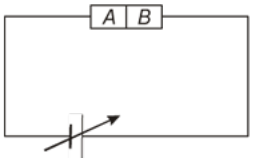
Q6. Pieces of copper and germanium are cooled from room temperature to 80 K. What will be the effect on their resistances?

Q7. Is the ratio of number of holes and the number of conduction electrons in an *n*-type extrinsic semiconductor more than, less than or equal to 1?

Q8. Doping of Se with Id leads to which type of semiconductor?

Q9. Give the ratio of the number of holes and the number of conduction electrons in an intrinsic semiconductor.

Q10. Two semiconductor materials, *A* and *B* shown in the given figure, are made by doping germanium crystal with arsenic indium, respectively. The two are joined and connected to a battery as shown.



(a) Will the junction be forward biased or reverse biased?

(b) Sketch a *V-I* graph for this arrangement.

Q11. Which of the statements given in Exercise 14.1 is true for *p*-type semiconductors.

Q12. C, Si and Ge have same lattice structure. Why is C insulator while Si and Ge intrinsic semiconductors?

Q13. In an *n*-type silicon, which of the following statement is true:

(a) Electrons are majority carriers and trivalent atoms are the dopants.

(b) Electrons are minority carriers and pentavalent atoms are the dopants.

(c) Holes are minority carriers and pentavalent atoms are the dopants.

(d) Holes are majority carriers and trivalent atoms are the dopants.

Q14. Can we take one slab of *p*-type semiconductor and physically join it to another *n*-type semiconductor to get *p-n* junction?

Q15. Determine the number of density of donor atoms which have to be added to an intrinsic germanium semiconductor to produce an *n*-type semiconductor of conductivity $5\Omega^{-1}\,cm^{-1}$. Given that the mobility of electrons in *n*-type Ge is $3{,}900\,cm^2\,V^{-1}\,s^{-1}$. Neglect the contribution of holes to conductivity.
Take charge on electron, $e = 1.6 \times 10^{-19}\,C$.

Q16. Pure Si at 300 K has equal electron(n_e) and hole (n_h) concentration of $1.5 \times 10^{16}\,m^{-3}$. Doping by indium increases n_h to $4.5 \times 10^{22}\,m^{-3}$. Calculate ne in the doped silicon.

Q17. Find the maximum wavelength of electromagnetic radiation, which can create a hole-electron pair in germanium. Given that forbidden energy gap in germanium is 0.72 eV.

Q18. Give the energy band diagram for (a) insulators, (b) metals and (c) semiconductors.

Q19. In a forward biased silicon diode, current occurs at close to 0.7 V and increases rapidly with very small further potential difference increase. What current will flow, when there is a $200\,\Omega$ resistor in series with the diode with a 10 V battery across the series combination?

Q20. What is meant by energy bands in solids? Draw labelled energy band diagrams to illustrate the behaviour of (a) a conductor; (b) a pure semi-conductor; and (c) an insulator.

Q21. With the help of energy band diagrams, distinguish between the conductors, insulators and semiconductors.

Q22. (a) Why silicon or germanium cannot be used in LEDs?
(b) Describe briefly with the help of a necessary circuit diagram, the working principle of a solar cell.

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S1. Resistance of a material can be found out by the slope of the curve V versus I. Part BC of the curve shows the negative resistance as with the increase in current and decrease as with the increase in current and decrease in voltage.

S2. The trivalent impurity atoms in a doped semiconductor accept electrons from the silicon crystal and therefore trivalent impurity is also called acceptor impurity.

S3. Silicon – 1.1 eV.

Ge – 0.72 eV

S4. Because at absolute zero (0 K) electrons do not have energies to move to conduction band and hence the semiconductors do not show any conductivity *i.e.*, semiconductors behave as insulators.

S5. It is because, all the bounds in a crystal get ruptured at a unique fixed temperature for that crystal. This fixed temperature is called the melting point of the crystal and is sharp in case of crystalline substances. At this fixed temperature, the crystal changes into the liquid state.

S6. Resistance of Ge will increase and that of Cu will decrease.

S7. It is less than 1.

S8. Doping of silicon with indium leads to get *p*-type semiconductor.

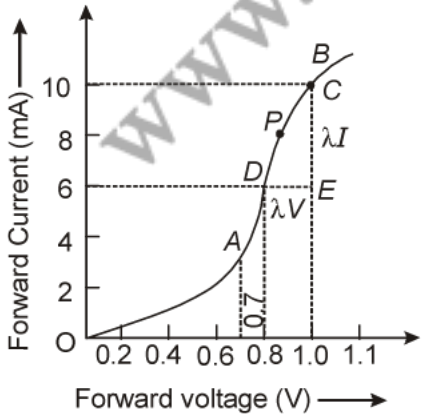
S9. It is 1.

S10. As is pentavalent and in is trivalent, so they produce *n* and *p*-type respectively.

Arsenic is pentavalent and indium is trivalent, so on dopping Germanium with Arsenic, *n*-type semiconductor will be formed.

(a) as, *A* (*n*-type) is connected with negative terminal and *B* (*p*-type) is connected with positive terminal of the battery so the junction is in forward bias.

(b) *V-I* graph



S11. The correct statement is **(d).**

In a *p*-type semiconductor, the holes are the majority carriers, while the electrons are the minority carriers. A p-type semiconductor is obtained when trivalent impurities, such as aluminium, are doped in silicon atoms.

S12. The 4 bonding electrons of C, Si or Ge lie, respectively, in the second, third and fourth orbit. Hence, energy required to take out an electron from these atoms (*i.e.*, ionisation energy E_g) will be least for Ge, followed by Si and highest for C. Hence, number of free electrons for conduction in Ge and Si are significant but negligibly small for C.

S13. The correct statement is **(c)**.

In an *n*-type silicon, the electrons are the majority carriers, while the holes are the minority carriers. An n-type semiconductor is obtained when pentavalent impurities, such as phosphorus, are doped in silicon atoms.

S14. No! Any slab, howsoever flat, will have roughness much larger than the inter-atomic crystal spacing (~2 to 3 Å) and hence *continuous contact* at the atomic level will not be possible. The junction will behave as a *discontinuity* for the flowing charge carriers.

S15. Given: $e = 1.6 \times 10^{-19}\,\text{C}$; $\sigma = 5\Omega^{-1}\,\text{cm}^{-1} = 500\Omega^{-1}\,\text{m}^{-1}$; $\mu_e = 3{,}900\ \text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1} = 0.39\,\text{m}^2\,\text{V}^{-1}\,\text{s}^{-1}$

Here, $\sigma = e n_e \mu_e$ (neglecting contribution of holes)

$\therefore$ $$n_e = \frac{\sigma}{e\mu_e}$$

$$= \frac{500}{1.6 \times 10^{-19} \times 0.39} = \mathbf{8.013 \times 10^{21}\,m^{-3}}.$$

S16. Given: $n_i = 1.5 \times 10^{16}\,\text{m}^{-3}$; $n_h = 4.5 \times 10^{22}\,\text{m}^{-3}$

Now, $n_e n_h = n_i^2$

$\therefore$ $$n_e = \frac{n_i^2}{n_h} \frac{(1.5 \times 10^{16})^2}{4.5 \times 10^{22}} = \mathbf{5 \times 10^{9}\,m^{-3}}.$$

S17. Given: $E_g = 0.72\,\text{eV} = 0.72 \times 1.6 \times 10^{-19}\,\text{J}$.

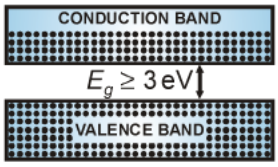
The maximum wavelength of radiation, which can create a hole-electron pair in germanium is given by

$$E_g = \frac{hc}{\lambda}$$

or $$\lambda = \frac{hc}{E_g} = \frac{6.62 \times 10^{-34} \times 3 \times 10^{8}}{0.72 \times 1.6 \times 10^{-19}}$$

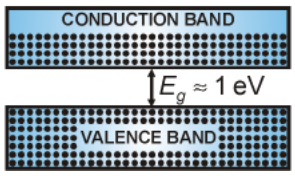
$$= \mathbf{1.724 \times 10^{-6}\,m}.$$

S18. (a)



(b)

(c)



S19. E.M.F. of the battery, $E = 10\,V$

Voltage drop across the junction diode, $v_d = 0.7\,V$

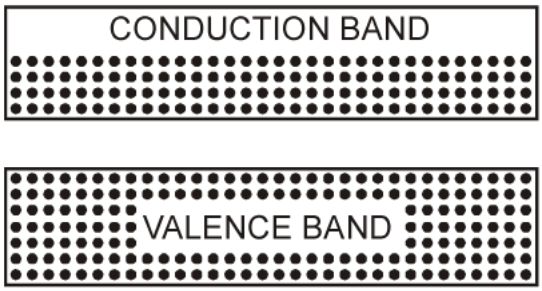
Therefore, voltage drop across the series resistor,

$$V = E - v_d = 10 - 0.7 = 9.3\,V$$

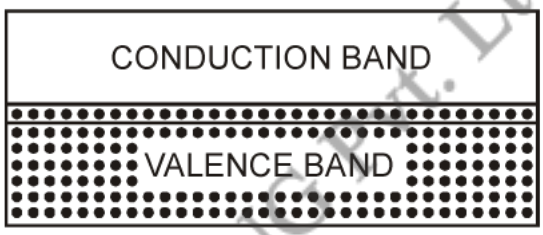
Hence, current in the circuit,

$$I = \frac{V}{R} = \frac{9.3}{200} = 4.65 \times 10^{-2}\,A = \mathbf{46.5\,mA}.$$

S20. (a)



(a)

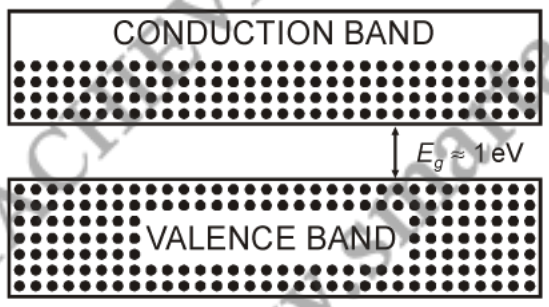


(b)

The valence band may be completely filled and the conduction band partially filled with an extremely small energy gap between them as shown in figure (a).

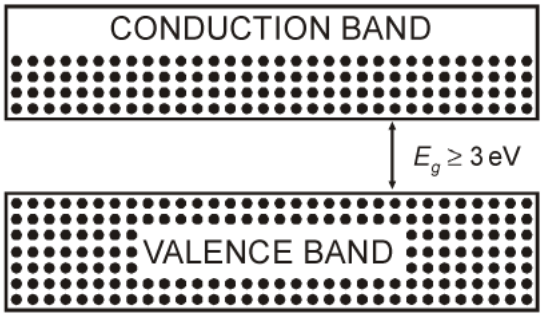
The valence band is completely filled and the conduction band is empty but the two overlap each other as shown in figure (b).

(b)



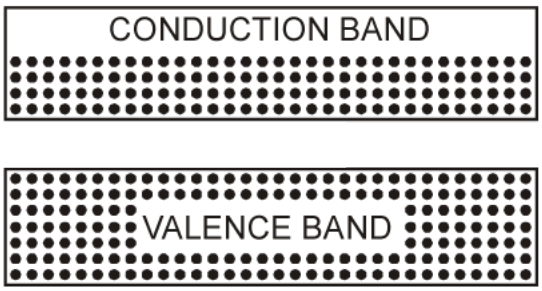
The energy gap between conduction band and valence band almost 1 eV in semiconductor material as shown in above figure.

(c)

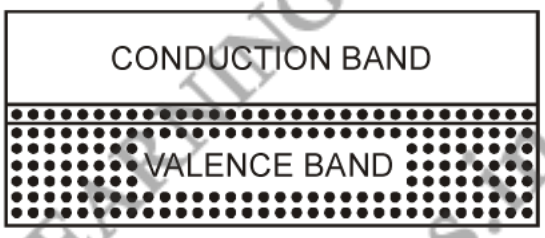


The energy gap between conduction band and valence band grater than 3 eV in insulator material as shown in above figure.

S21. **Conductors (Metals):** In metallic conductors either the conduction band is partially filled [as shown in figure (a)] as in case of Na, Li, K, etc. or there is partial overlapping of conduction band and valence band [as shown in figure (b)] as in case of Zn, Mg, Be, etc. In both the situations large number of free electrons are available in the conduction band. Therefore, on applying even a small electric field, the metals conduct electricity. Thus, metals are good conductors of electricity.

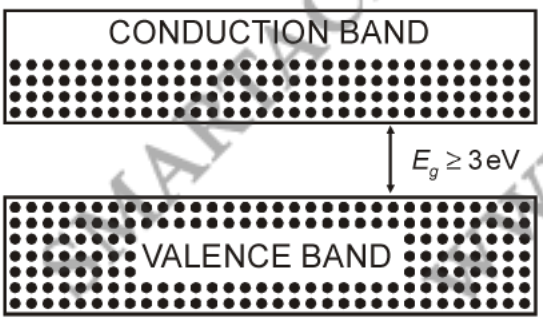


(a)

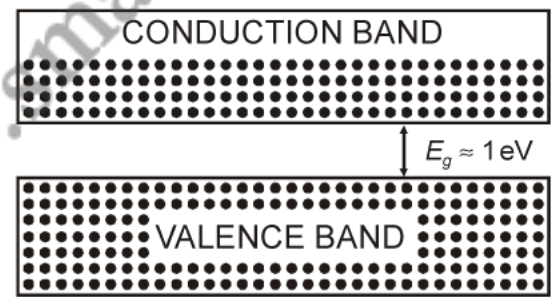


(b)

Insulators: In insulators the unfilled conduction band is separated from the filled valence band by aforbidden gap of energy 3 eV or more [as shown in figure (c)]. This means that a minimum of 3 eV energy is required by an electron to jump to the conduction band.



(c)



(d)

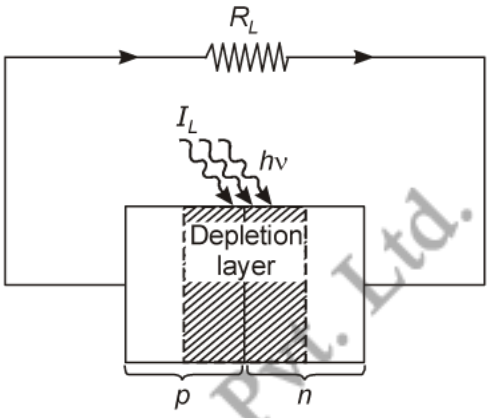
When electric field is applied across such a solid, the electrons find it difficult to acquire such a large amount of energy and so the conduction band continues to be empty and hence no current flows through it.

Semiconductors: The energy band structure of the semiconductors is similar to the insulators but with a smaller forbidden gap energy of about 1 eV [as shown in figure (d)]. The forbidden gap energy is 0.785 eV for germanium and 1.21 eV for silicon. At 0 K, electrons are not able to cross even this small forbidden gap and hence the conduction band remains totally empty. Therefore,

at 0 K, semiconductors behave as insulators. However, at room temperature, some electrons in the valence band acquire enough energy to crossover to the conduction band where they are free to move under an applied electric field constituting an electric current. As a result of it, the semiconductor shows a small conductivity at room temperature.

S22. (a) Because of their low values of E_g.

(b) When light of frequency, ν such that $h\nu > E_g$ (band gap) is incident on junction, then electron-hole pair liberated in the depletion region drifts under the influence of potential barrier. The gathering of these charge carriers make *p*-type as positive electrode and *n*-type as negative electrode and hence generating photo-voltage across solar cell.



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Q1. How does the energy gap of an intrinsic semiconductor vary, when doped with a trivalent impurity.

Q2. Draw the energy-band diagram for a *p*-type semiconductor.

Q3. Draw energy-band diagram for an *n*-type extrinsic semiconductor.

Q4. Draw an energy-band diagram for an intrinsic semi-conductor.

Q5. In an unbiased *p*-*n* junction, holes diffuse from the *p*-region to *n*-region because

(a) free electrons in the *n*-region attract them.

(b) they move across the junction by the potential difference.

(c) hole concentration in *p*-region is more as compared to *n*-region.

(d) All the above.

Q6. Carbon, silicon and germanium have four valence electrons each. These are characterised by valence and conduction bands separated by energy band gap respectively equal to $(E_g)_C$, (*Eg*)Si and (*Eg*)Ge. Which of the following statements is true?

(a) $(E_g)_{Si} < (E_g)_{Ge} < (E_g)_C$ (b) $(E_g)_C < (E_g)_{Ge} > (E_g)_{Si}$

(c) $(E_g)_C > (E_g)_{Si} > (E_g)_{Ge}$ (d) $(E_g)_C = (E_g)_{Si} = (E_g)_{Ge}$

Q7. What happens to the width of depletion layer of a *p*-*n* junction when it is

(a) forward biased? (b) reverse biased?

Q8. Distinguish between intrinsic and extrinsic semiconductors.

Q9. What types of charged carries are there in an *n*-type semiconductor?

Q10. What type of impurities do you add to a silicon crystal to obtain *n*-type and *p*-type semiconductors?

Q11. Why mobility of holes is less than that of free electrons?

Q12. In the figure below, is the diode *D* forward or reverse biased?

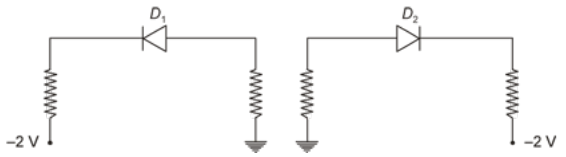
Q13. In the figure below, is the diode *D* forward or reverse biased?

Q14. How does conductivity of a semiconductor change with rise in temperature?

Q15. Which one of the two diodes, D_1 and D_2 in the given figure is

(a) forward biased?

(b) reverse biased?



Q16. Distinguish between an intrinsic semiconductor and *p*- type semiconductor.

Q17. Suppose a pure Si crystal has 5×10^{28} atoms m^{-3}. It is doped by 1 ppm concentration of pentavalent As. Calculate the number of electrons and holes. Given that $n_i = 1.5 \times 10^{16} m^{-3}$.

Q18. Distinguish between *n*-type and *p*-type semiconductors on the basis of energy band diagram.

Q19. For an extrinsic semiconductor, indicate on the energy band diagram the donor and acceptor levels.

Q20. Explain the effect of temperature variation on the resistivity of pure semiconductors.

Q21. The mean free path of conduction electrons in copper is about 4.2×10^{-8} m. Find the electric field which can give 2.4 eV energy (on the average) to a conduction electron in a copper block.

Q22. The number of silicon atoms per m^3 is 5×10^{28}. This is doped simultaneously with 5×10^{22} atoms per m^3 of Arsenic and 5×10^{20} per m^3 atoms of Indium. Calculate the number of electrons and holes. Given that $n_i = 1.5 \times 10^{16} m^{-3}$. Is the material *n*-type or *p*-type?

Q23. In an intrinsic semiconductor the energy gap E_g is 1.2 eV. Its hole mobility is much smaller than electron mobility and independent of temperature. What is the ratio between conductivity at 600 K and that at 300 K? Assume that the temperature dependence of intrinsic carrier concentration n_i is given by

$$n_i = n_0 \exp\left[-\frac{E_g}{2k_B T}\right]$$

where n_0 is a constant.

Q24. Distinguish between intrinsic and extrinsic semiconductors?

Q25. (a) Draw the typical shape of the *V-I* characteristics of a *p-n* junction diode both in (a) forward (b) reverse bias configuration. How do we infer, from these characteristics that a diode can be used to rectify alternating voltages?

(b) Draw the circuit diagram of a full wave rectifier using a centre-tap transformer and two *p-n* junction diodes. Give a brief description of the working of this circuit.

Q26. (a) Explain the formation of 'depletion layer' and 'barrier potential' in *p-n* junction.

(b) With the help of a lebelled circuit diagram explain the use of a *p-n* junction diode as a full wave rectifier. Draw the input and output waveforms.

Q27. (a) Draw a circuit arrangement for studying *V-I* characteristics of a *p-n* junction diode in
(i) forward bias and (ii) reverse bias
Show the typical *V-I* characteristics of a silicon dioade.

(b) State the main practical application of LED.

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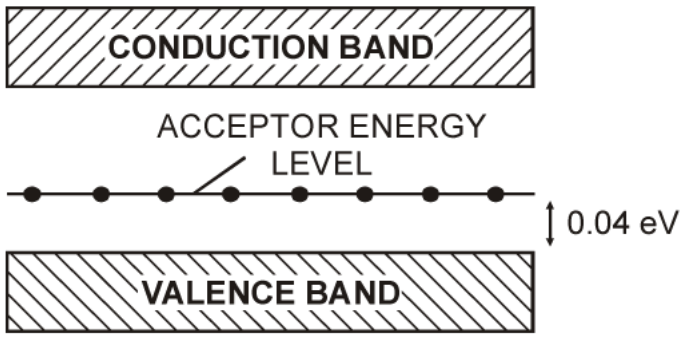
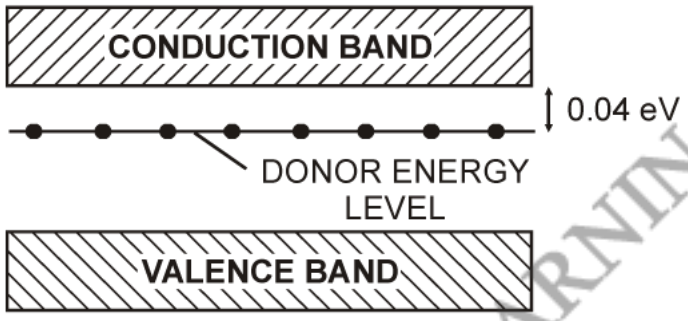
S1. When a trivalent impurity is added to an intrinsic semiconductor, an acceptor energy level is created in the forbidden energy gap just above the valence band. Due to this, electrons from the valence band are easily transferred to the acceptor energy level.

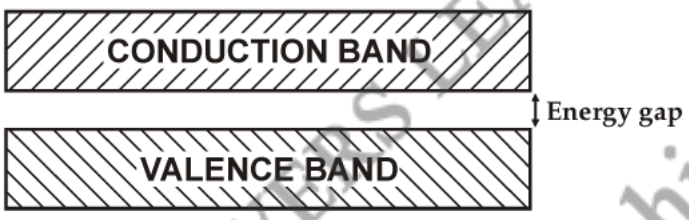
S2.



S3.



S4.



S5. The correct statement is **(c)**.

The diffusion of charge carriers across a junction takes place from the region of higher concentration to the region of lower concentration. In this case, the *p*-region has greater concentration of holes than the *n*-region. Hence, in an unbiased *p*-*n* junction, holes diffuse from the *p*-region to the *n*-region.

S6. The correct statement is **(c)**.

Of the three given elements, the energy band gap of carbon is the maximum and that of germanium is the least.

The energy band gap of these elements are related as: $(E_g)_C > (E_g)_{Si} > (E_g)_{Ge}$

S7. (a) Width of depletion layer's decreases in forward bias.

(b) Width depletion layer increases in reverse bias.

S8. Intrinsic semiconductors means pure while extrinsic means doped (*n*-type or *p*-type).

S9. Negative charge carriers (electrons).

S10. To obtain *n*-type semiconductor, pentavalent impurity is added.

To obtain *p*-type semiconductor, trivalent impurity is added.

S11. It is due to smaller drift velocity (v_d) acquired by the holes; Less drift velocity makes mobility $\mu = v/E$ less for same electric field E.

S12. Since, *n*-section is connected to positive terminal of the battery, the diode is *reverse biased*.

S13. Since *n*-section is connected to earth and *p*-section is at – 10 V, the diode is *reverse biased*.

S14. The conductivity of a semiconductor increases with temperature.

S15. In forward bias, *p*-type end is at higher (or positive) potential and *n*-type end is at lower (or negative) potential.

(a) D_2 is in forward bias become *p*-type is at higher potential (0) as compared to *n*-type (–2 V).

(b) D_1 is in reverse bias because *p*-type is a lower potential (–2 V) as compared to *n*-type (0 V).

S16. Distinguish between an intrinsic semiconductor and *p*- type semiconductor as follows:

intrinsic semiconductor	*p*- type semiconductor
1. Examples of intrinsic semiconductors are crystalline from of pure silicon and germanium.	1 The holes are majority carriers and electrons are minority carriers.
2. The number of electrons in conduction band is equal to the number of holes in valence band.	2. The trivalent impurity atoms, called acceptor atoms, are the source of holes (vacant electron sites).

S17. Note that thermally generated electrons ($n_i \sim 10^{16}\ m^{-3}$) are negligibly small as compared to those produced by doping.

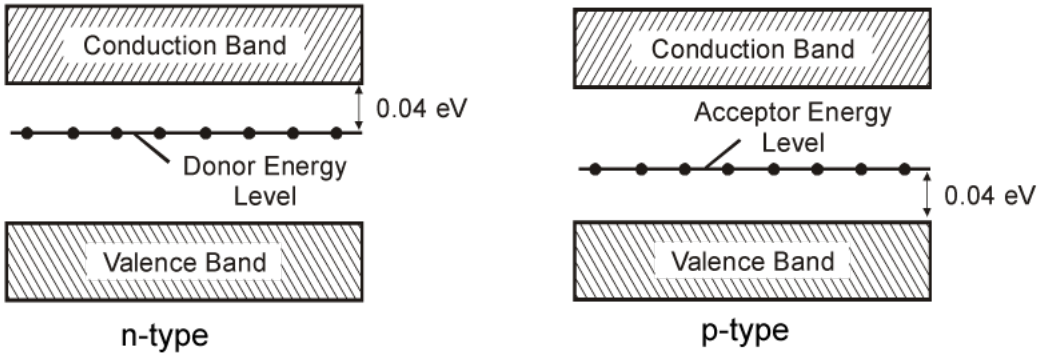
Therefore, $n_e \approx N_D$.

Since, $n_e n_h = n_i^2$,

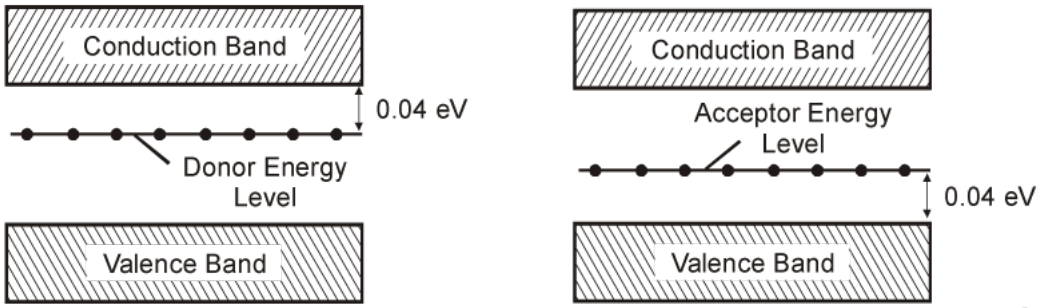
The number of holes $n_h = (2.25 \times 10^{32})/(5 \times 10^{22})$

$\sim 4.5 \times 10^9\ m^{-3}$.

S18.



S19.



S20. The variation in the resistivity of a pure semiconductor is mainly due to the change in carrier concentration. The fraction of the number of electrons raised from the valence band to the conduction band is given by

$$f \propto e^{-E_g/kT}$$

It follows that as temperature (T) increases, the value of fraction f also increases *i.e.*, conductivity of the semiconductor increases. In other words, as temperature of the semi conductor increases, its resistivity decreases.

S21. Let E be the required electric field. Then, force on electron due to electric field,

$$F = eE = 1.6 \times 10^{-19} E$$

The work done by the electric field on the electron, before it collides with a copper iron (or atom),

$$W = F \times \text{mean free path} = 1.6 \times 10^{-19} E \times 4.2 \times 10^{-8}$$

$$= 6.72 \times 10^{-27} E \text{ (in joule)}$$

$$= \frac{6.72 \times 10^{-27} E}{1.6 \times 10^{-19}} = 4.2 \times 10^{-8} E \text{ (in eV)}$$

$\therefore$ $4.2 \times 10^{-8} E = 2.4$

or $E = \mathbf{5.71 \times 10^{7}\ Vm^{-1}}$.

S22. Number of silicon atoms, $N = 5 \times 10^{28}$ atoms/m^3

Number of arsenic atoms, $n_{As} = 5 \times 10^{22}$ atoms/m^3

Number of indium atoms, $n_{In} = 5 \times 10^{20}$ atoms/m^3

Number of thermally-generated electrons, $n_i = 1.5 \times 10^{16}$ electrons/m^3

Number of electrons, $n_e = 5 \times 10^{22} - 1.5 \times 10^{16} \approx 4.99 \times 10^{22}$

Number of holes = n_h

In thermal equilibrium, the concentrations of electrons and holes in a semiconductor are related as:

$$n_e n_h = n_i^2$$

$$\therefore \quad n_h = \frac{n_i^2}{n_e}$$

$$= \frac{(1.5 \times 10^{16})^2}{4.99 \times 10^{22}} \approx 4.51 \times 10^9$$

Therefore, the number of electrons is approximately 4.99×10^{22} and the number of holes is about 4.51×10^9. Since the number of electrons is more than the number of holes, the material is an *n*-type semiconductor.

S23. Energy gap of the given intrinsic semiconductor, $Eg = 1.2$ eV

The temperature dependence of the intrinsic carrier-concentration is written as:

$$n_i = n_0 \exp\left[-\frac{E_g}{2k_B T}\right]$$

Where, k_B = Boltzmann constant = 8.62×10^{-5} eV/K

T = Temperature

n_0 = Constant

Initial temperature, $T_1 = 300$ K

The intrinsic carrier-concentration at this temperature can be written as:

$$n_{i1} = n_0 \exp\left[-\frac{E_g}{2k_B \times 300}\right] \quad \ldots \text{(i)}$$

Final temperature, $T_2 = 600$ K

The intrinsic carrier-concentration at this temperature can be written as:

$$n_{i2} = n_0 \exp\left[-\frac{E_g}{2k_B \times 600}\right] \quad \ldots \text{(ii)}$$

The ratio between the conductivities at 600 K and at 300 K is equal to the ratio between the respective intrinsic carrier-concentrations at these temperatures.

$$\frac{n_{i2}}{n_{i1}} = \frac{n_0 \exp\left[-\frac{E_g}{2k_B 600}\right]}{n_0 \exp\left[-\frac{E_g}{2k_B 300}\right]}$$

$$= \exp \frac{E_g}{2k_B}\left[\frac{1}{300} - \frac{1}{600}\right] = \exp\left[\frac{1.2}{2 \times 8.62 \times 10^{-5}} \times \frac{2-1}{600}\right]$$

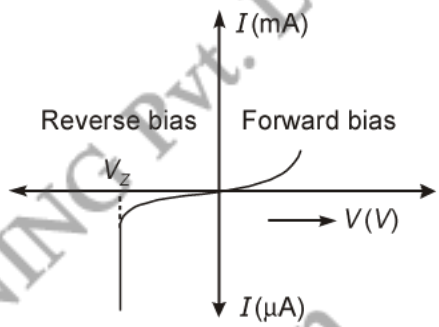
$$= \exp [11.6] = 1.09 \times 10^5$$

Therefore, the ratio between the conductivities is 1.09×10^5.

S24. A semiconductor free from all types of impurities is called an intrinsic semiconductor. At room temperature, a few covalent bonds break up and the electrons come out. In the bonds, from which electrons come out, vacancies are created. These vacancies in covalent bonds are called holes. In an intrinsic semiconductor, holes and electrons are equal in number and they are free to move about in the semiconductor.

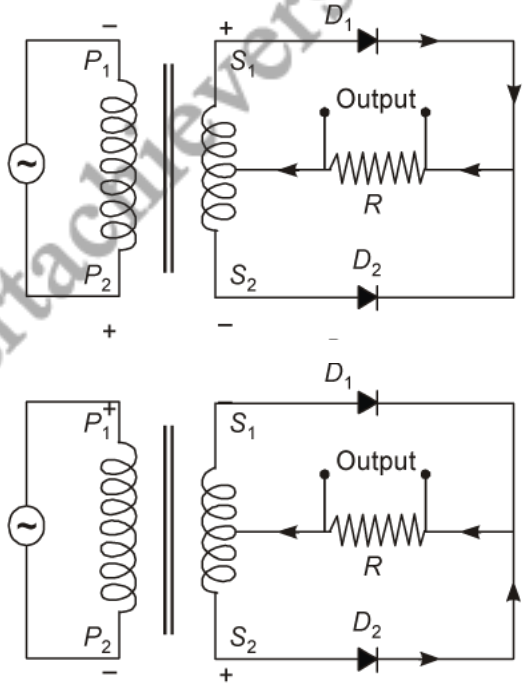
On the other hand, a semiconductor doped with a suitable impurity (donor or acceptor), so that it possesses conductivity much higher than that of pure semiconductor, is called an extrinsic semiconductor. The extrinsic semiconductor may be of *n*-type or *p*-type.

S25. (a) *V-I* characteristics of *p-n* junction diode both in forward reverse bias



From these two graphs we see that the junction diodes operates mainly in forward diodes operates mainly in forward bias, this characteristics of junction diode can be used to make it a rectifier.

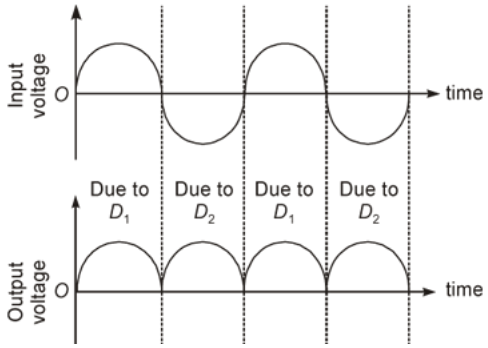
(b) ***Full-wave rectifier:*** The circuit diagram of a full-wave rectifier is shown in figure. The a.c. to be rectified is fed to the primary terminals of a centre-tapped transformer.



During the first (positive) half cycle of the a.c. input, the upper end of the secondary coil acquires positive potential and the lower end acquires negative potential. As a result, diode D_1 gets forward biased and diode D_2 gets reverse biased. Diode D_1 conducts and a current flows through load, as shown by continuous in Figure.

During the next (negative) half cycle of the a.c. input, the upper end of the secondary coil acquaires negative potential and the lower end acquires positive potential. As a result, diode D_1 gets reverse biased and diode D_2 gets forward biased. Diode D_2 conducts and a current flows through load, as shown by dotted lines in figure. The direction of current remains same as in the previous half cycle.

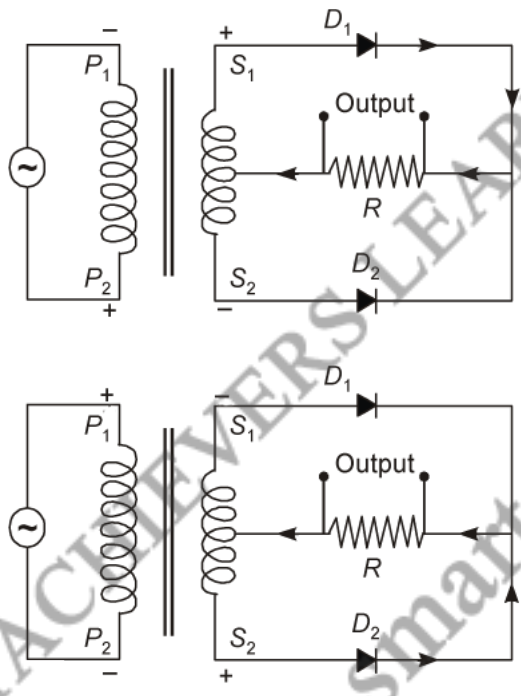
The input and output waveforms have been given below.



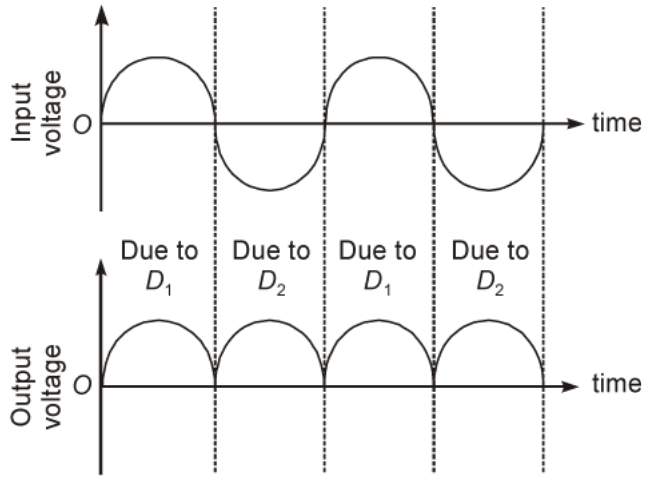
Its working based on the principle that junction diode offer very low resistance in forward bias and very high resistance in reverse bias.

S26. (a) With the formation of *p*-*n* junction, the holes from *p*-region and electron-hole pair combine and get annihilated. This in turn, produces potential barrier, V_R across the junction which opposes the further diffusion through the junction. Thus, small region forms in the vicinity of the junction which is depleted of free charge carrier and has only immotile ions is called the depletion region.

(b) The circuit diagram of full wave rectifier is shown below.

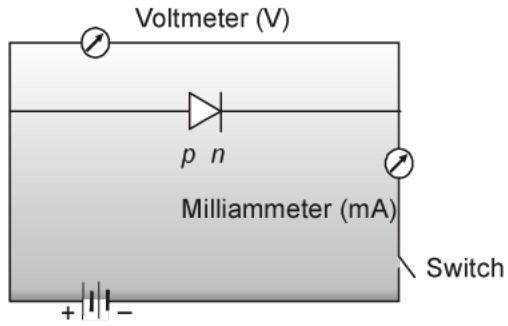


The input and output waveforms have been given below.

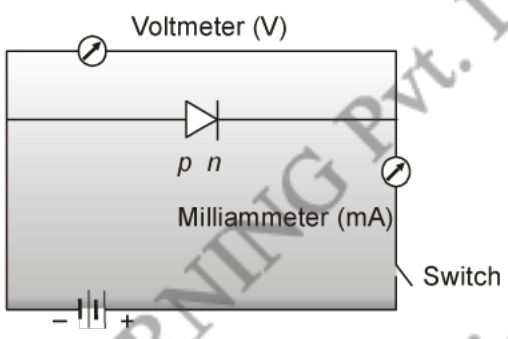


Its working based on the principle that junction diode offer very low resistance in forward bias and very high resistance in reverse bias.

S27. (a)

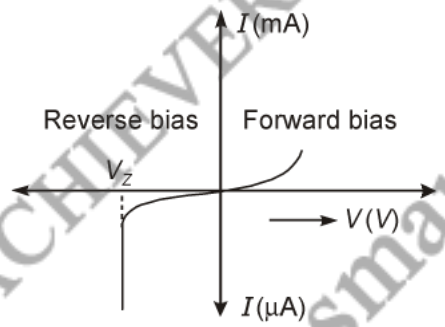


Circuit digram for p-n junction diode in forward bias



Circuit digram for p-n junction diode in reversce bias

V-I characteristics of a silicon dioade.



(b) LEDs are frequently used as pilot lights in electronic appliances to indicate whether the circuit is closed or not.

LEDs are used to illuminate the traffic signal lighting.

LEDs are used in numeric displays (in digital watches and calculators).

LEDs are also used in picture phones (to sense images) and video displays.

LEDs are used in optical mouses for the computers. They are also used in computer memories and optical communcation.

Date: 22/10/2021

Q1. What do you mean by rectification?

Q2. What is the direction of diffusion current in a junction diode?

Q3. In the depletion region of an unbiased *p-n* junction diode, what are the charge carriers?

Q4. Draw the voltage current characteristic of a zener diode.

Q5. Which biasing will make the resistance of a *p-n* junction high?

Q6. A *p-n* junction diode conducts when it is _____ biased.

Q7. Name the diode, (a) for which the output voltage is a regulated voltage. (b) that emits spontananeous radiation, when forward biased.

Q8. How reverse current suddenly increases at the break down voltage in case of a junction diode?

Q9. Draw circuit diagram of a *p-n*-junction with reverse bias.

Q10. Which type of biasing gives a semiconductor diode very high resistance?

Q11. How does the junction width change, when a *p-n*-junction is forward biased?

Q12. What is depletion region in a *p-n*-junction?

Q13. When a forward bias is applied to a *p-n* junction, it

(a) raises the potential barrier
(b) reduces the majority carrier current to zero
(c) lowers the potential barrier
(d) None of the above

Q14. Can two separate *p-n* junction diodes be used to form a transistor?

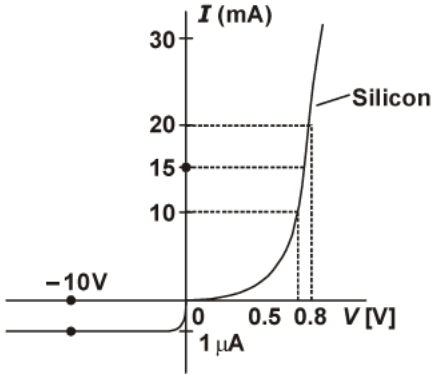
Q15. Why cannot we take one slab of *p*-type semiconductor and physically join it to another slab of *n*-type semiconductor to get *p-n* junction?

Q16. What is the most common use of photodiode?

Q17. In half-wave rectification, what is the output frequency if the input frequency is 50 Hz. What is the output frequency of a full-wave rectifier for the same input frequency.

Q18. A *p-n* photodiode is fabricated from a semiconductor with band gap of 2.8 eV. Can it detect a wavelength of 6000 nm?

Q19. The *V-I* characteristic of a silicon diode is shown in the figure. Calculate the resistance of the diode at (a) I_D = 15 mA and (b) V_D = – 10 V.

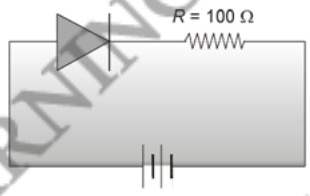


Q20. In a Zener regulated power supply a Zener diode with V_Z = 6.0 V is used for regulation. The load current is to be 4.0 mA and the unregulated input is 10.0 V. What should be the value of series resistor R_S?

Q21. The current in the forward bias is known to be more (~ mA) than the current in the reverse bias (~ μA). What is the reason then to operate the photodiodes in reverse bias?

Q22. Why are Si and GaAs are preferred materials for solar cells?

Q23. Figure shows a junction diode connected to an external resistance of 100Ω and a source of e.m.f. of 3.0 V. Assuming that the barrier potential developed in the junction diode is 0.7 V, obtain the current in the circuit.

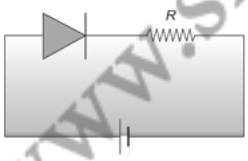


Q24. How does the width of the depletion region of a *p-n* junction vary, if the reverse bias applied to it increases?

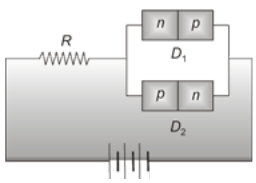
Q25. Draw the energy band diagram of *n*-type semiconductor. How does the forbidden energy gap of an intrinsic semiconductor vary with increase in temperature?

Q26. Draw the energy band diagram of a *p*-type semiconductor. How does the forbidden energy gap of an intrinsic semiconductor vary with increase in temperature?

Q27. A diode used in the circuit shown in the figure below, has a constant voltage drop of 0.5 V at all currents and a maximum power rating of 100 mW. What should be the value of the resistance *R* connected in series with diode for obtaining maximum current?



Q28. The figure shows two *p-n* junctions diodes along with a resistance *R* and a d.c. battery *E*.
Indicate the path and direction of flow of appreciable current in the circuit.

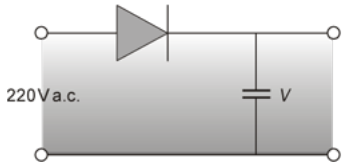


Q29. A full-wave rectifier makes use of two identical junction diodes having negligible forward resistance. Find the r.m.s. value of voltage across R_L, when a sinusoidal voltage supply of peak value 100 V is fed to the rectifier.

Q30. The current in the forward bias is known to be more (≈ mA) than the current in the reverse bias (≈ μA). What is the reason, then, to operate the photodiode in reverse bias.

Q31. Name the *p-n* junction diodes which emit spontaneous radiation, when forward biased. How do we choose the semiconductor, to be used in these diodes, if the emitted radiation, is to be in the visible region.

Q32. A diode is connected to 220 V (r.m.s.) a.c. in series with a capacitor as shown in the figure. What is the voltage *V* across the capacitor?



Q33. The following table provides the set of values, of *V* and *I*, obtained for a given diode:

Forward biasing		Reverse biasing	
V	*I*	*V*	*I*
2 V	60 mA	0 V	0 μA
2.4 V	80 mA	– 2 V	– 0.25 μA

Assuming the characteristics to be nearly linear, over this range, calculate the forward and reverse bias resistance of the given diode.

Q34. Draw the circuit diagram showing how a *p-n* junction diode is
(i) forward biased, (ii) reverse biased.
How is the width of depletion layer affected in the two cases?

Q35. Explain, how a depletion region is formed in a junction diode?

Q36. How is forward biasing different from reverse biasing in a *p-n* junction diode?

Q37. Name the semiconductor device that can be used to regulate an unregulated DC power supply. With the help of *I-V* characteristics of this device, explain its principle.

Q38. The current in the forward bias is known to be more (~ mA) then the current in the reverse bias (~ μA). What is the reason, to operate the photodiode in reverse bias?

Q39. In the circuit using a sender diode voltage stabiliser (shown in the figure below), what is the smallest value of load resistance for stabilisation to be possible. Given, $R = 100\ \Omega$, $E = 5$ V and Zender diode is of 3 V.

Q40. How is that the reverse current in a Zener diode start increasing suddenly at a relatively low breakdowns voltage of 5 V or so?

Q41. Write the main use of the (a) photo diode (b) Zener diode.

Q42. Draw the circuit diagram of an illuminated photodiode in reverse bias. How is photodiode used to measure light intensity?

Q43. In a *p-n* junction diode, the current I can be expressed as

$$I = I_0 \exp\left(\frac{eV}{2k_BT} - 1\right)$$

where I_0 is called the reverse saturation current, V is the voltage across the diode and is positive for forward bias and negative for reverse bias, and I is the current through the diode, k_B is the Boltzmann constant (8.6×10^{-5} eV/K) and T is the absolute temperature. If for a given diode $I_0 = 5 \times 10^{-12}$ A and $T = 300$ K, then

(a) What will be the forward current at a forward voltage of 0.6 V?

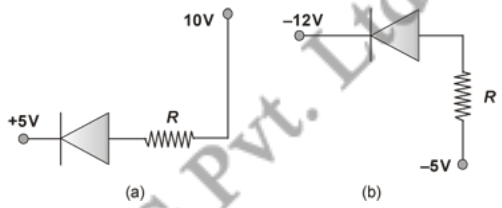
(b) What will be the increase in the current if the voltage across the diode is increased to 0.7 V?

(c) What is the dynamic resistance?

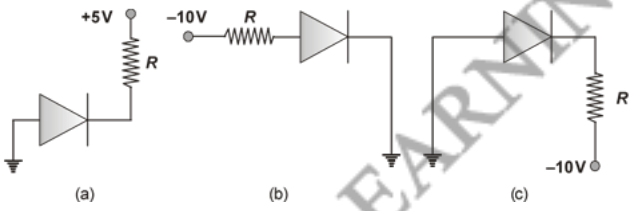
(d) What will be the current if reverse bias voltage changes from 1 V to 2 V?

O44. What are 'holes'? Write their characteristics.

Q45. In the following circuits, which of the diodes is forward biased and which is reverse biased?



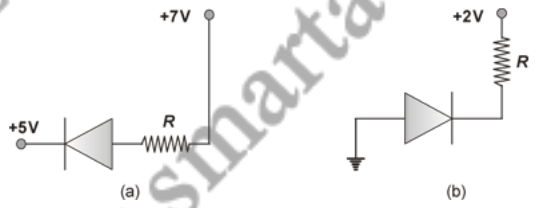
Q46. In the following circuits, which of the diodes is forward-biased and which is reverse-biased and why?



Q47. What do you by depletion region and potential barrier in a junction diode?

Q48. How is *n*-type semiconductor formed? Name the majority charge carriers in ti. Draw the energy band diagram of an *n*-type semiconductor.

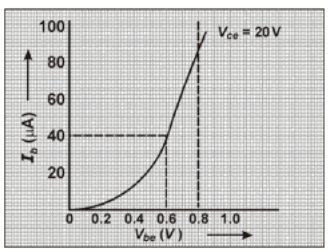
Q49. In the following diagrams, indicate which of the diodes are forward biased and which are reverse biased.



Q50. The figure shows the variation of I_b as a function of V_{be} at fixed $V_{ac} = 20$ V.

(a) Find the voltage corresponding to $I_b = 40$ mA and 847 mA;

(b) Find the resistance $R = V_{be}/I_b$ at these two points and the dynamic resistance.



Q51. Refer to the zener diode circuit shown in the figure. If $E = 12$ V, $V_Z = 9$ V, $R = 200\ \Omega$ and $R_L = 1.5$ kΩ. Calculate the power dissipated in (a) resistance R (b) load resistance R_L and (c) the zener diode.

Q52. State the main practical application of LED. Explain, giving reason, why the semiconductor used for the fabrication of visible light LEDs must have a band gap of atleast (nearly) 1.8 eV.

Q53. What is light emitting diode (LED)? Draw a circuit diagram and explain its working.

Q54. Which special type of diode can act as a voltage regulator? Give the symbol of this diode and draw the general shape of its *V-I* characteristics.

Q55. (a) Why is a photodiode operated in reverse bias mode?
(b) Why is the base region of a transistor made very thin and lightly doped?
(c) How does the collector current change in a junction transistor, if the base region has larger width?

Q56. How is a Zener diode fabricated so as to make it a special purpose semiconductor diode? Draw the circuit diagram of a Zener diode as a voltage regulator and explain its working.

Q57. A junction diode of negligible forward resistance is used as a half-wave rectifier to rectify a sinusoidal voltage supply 30 V (r.m.s.), 50 Hz. The output is obtained across a load resistance R_L of 10 kΩ. Calculate (a) the peak value of output current, (b) the reading of d.c. milliameter connected in series to R_L and (c) the reading of the d.c. voltmeter connected across a capacitor of 16 μF connected in parallel to R_L.

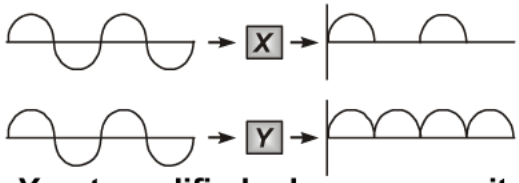
Q58. Draw a labelled diagram of a full wave rectifier circuit. State its working principle. Show the input-output waveforms.

Q59. Draw *V-I* characteristics of a *p-n* junction diode. Answer the following questions, giving reasons.
(a) Why is the current under reverse bias almost independent of the applied potential up to a critical voltage?
(b) Why does the reverse current show a sudden increase at the critical voltage?
Name any semiconductor device which operates under the reverse bias in the breakdown region.

Q60. (a) Draw the circuit diagrams of a *p-n* junction diode in (i) forward bias, (ii) reverse bias. How are these circuits used to study the *V – I* characteristics of a silicon diode? Draw the typical *V – I* characteristics.
(b) What is a light emitting diode (LED)? Mention two important advantages of LEDs over conventional lamps.

Q61. (a) Describe briefly, with the help of a diagram, the role of the two important processes involved in the formation of a *p-n* junction.
(b) Name the device which is used as a voltage regulator. Draw the necessary circuit diagram and explain its working.

Q62. An a.c. signal is fed into two circuits '*X*' and '*Y*' and the corresponding output in the two cases have the waveforms as shown.

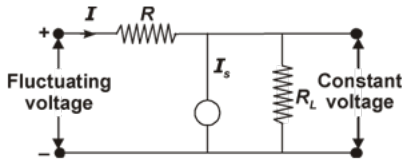


(a) Identify the circuits '*X*' and '*Y*'. Draw their labelled circuit diagrams.
(b) Briefly explain the working of circuit *Y*.
(c) How does the output waveform from circuit *Y* get modified when a capacitor is connected across the output terminals parallel to the load resistor?

Q63. Why is a Zener diode considered as a special purpose semiconductor diode? Draw the *I-V* characteristics of Zener diode and explain briefly how reverse current suddenly increase at the breakdown voltage?

Describe briefly with the help of a circuit diagram how a Zener diode works to obtain a constant DC voltage from the unregulated DC output of a rectifier.

Q64. (a) Name the device, D which is used as a voltage regulator in the given circuit and give its symbol.



(b) Explain briefly, with the help of a circuit diagram, how a *p-n* junction diode works as a half wave rectifier.

Q65. (a) Draw *V – I* characteristics of a Zener diode.

(b) Explain with the help of a circuit diagram, the use of a Zener diode as a voltage regulator.

(c) A photodiode is operated under reverse bias although in the forward bias the current is known to be more than the current in the reverse bias. Explain, giving reason.

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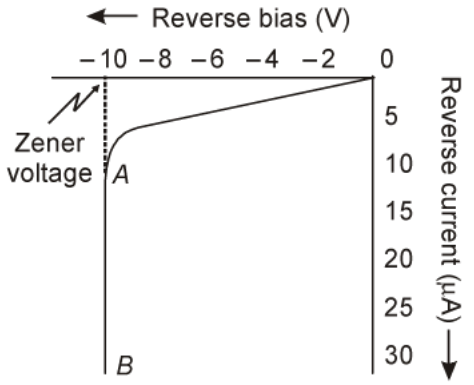
S1. Rectification is the process of conversion of alternating current into direct current.

S2. In junction diode, the direction of diffusion current is from *p*-region to *n*-region.

S3. In the depletion region of an unbiased *p-n* junction diode, there are only fixed ions but no free charge carriers.

S4.



In the above figure shows the reverse bias characteristic of a *p-n* junction in general. Zener diodes are designed to operate in the reverse-current breakdown region. They can be operated in this region without any damage to them. The part *AB* of *ht* reverse bias characteristic (beyond zener breakdown voltage) represents the *V-I* characteristic of a zener diode.

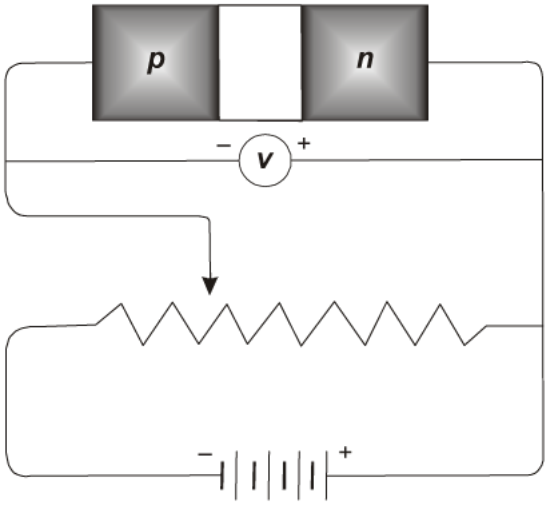
S5. "Reverse".

S6. Forward.

S7. (a)Zener diode (b) Photodiode.

S8. When the reverse voltage exceeds the zener voltage, the valence electrons break free under the influence of the electric field due to the applied voltage and the diode conducts a large current in the reverse direction. It is called is Zener-break down.

S9.



S10. Reverse biasing.

S11. The junction width decreases, when a *p*-*n*-junction is forward biased.

S12. A thin layer between *p*- and *n*-sections of the junction diode, devoid of free electrons and holes, is called depletion layer.

S13. The correct statement is **(c)**.

When a forward bias is applied to a *p*-*n* junction, it lowers the value of potential barrier. In the case of a forward bias, the potential barrier opposes the applied voltage. Hence, the potential barrier across the junction gets reduced.

S14. No, because in such a case, the region which will form the base will be too thick.

S15. In this way, continuous contact cannot be produced at atomic level and junction will be have as a discontinuity for the flowing charge carrier.

S16. The photodiode can be used as a photodetector detect optical signals.

S17. Input frequency = 50 Hz

For a half-wave rectifier, the output frequency is equal to the input frequency.

$\therefore$ Output frequency = 50 Hz

For a full-wave rectifier, the output frequency is twice the input frequency.

$\therefore$ Output frequency = $2 \times 50 = 100$ Hz. [Output is obtained both during – ve and + ve half cycle]

S18. Energy band gap of the given photodiode, $E_g = 2.8$ eV

Wavelength, $\lambda = 6000$ nm $= 6000 \times 10^{-9}$ m

The energy of a signal is given by the relation:

$$E = \frac{hc}{\lambda}$$

Where, h = Planck's constant $= 6.626 \times 10^{-34}$ Js

c = Speed of light = 3×10^8 m/s

$$E = \frac{6.626 \times 10^{-34} \times 3 \times 10^8}{6000 \times 10^{-9}} = 3.313 \times 10^{-20} \text{ J}$$

But 1.6×10^{-19} J = 1 eV

$\therefore$ $E = 3.313 \times 10^{-20}$ J

$$= \frac{3.313 \times 10^{-20}}{1.6 \times 10^{-19}} = 0.207 \text{ eV}$$

The energy of a signal of wavelength 6000 nm is 0.207 eV, which is less than 2.8 eV – the energy band gap of a photodiode. Hence, the photodiode cannot detect the signal.

S19. Considering the diode characteristics as a straight line between I = 10 mA to I = 20 mA passing through the origin, we can calculate the resistance using Ohm's law.

(a) From the curve, at I = 20 mA, V = 0.8 V, I = 10 mA, V = 0.7 V

$r_{fb} = \Delta V/\Delta I$ = 0.1V/10 mA = 10 W

(b) From the curve at V = – 10 V, I = – 1 μA,

Therefore, r_{rb} = 10 V/1 μA = 1.0×10^7 Ω.

S20. The value of R_S *i.e.*, resistor in series should be such that the current through the Zener diode is much larger than the load current. This is to have good load regulation. Choose Zener current as five times the load current, *i.e.*, I_Z = 20 mA. The total current through R_S is, therefore, 24 mA. The voltage drop across R_S is 10.0 – 6.0 = 4.0 V. This gives $R_S = 4.0\text{V}/(24 \times 10^{-3})\text{A} = 167\ \Omega$. The nearest value of carbon resistor is 150 Ω. So, a series resistor of 150 Ω is appropriate. Note that slight variation in the value of the resistor does not matter, what is important is that the current I_Z should be sufficiently larger than I_L.

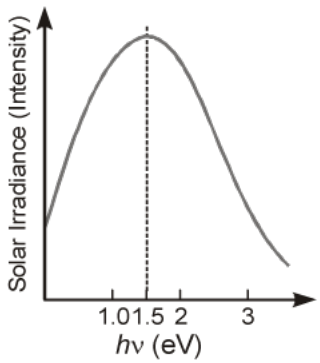
S21. Consider the case of an *n*-type semiconductor. Obviously, the majority carrier density (n) is considerably larger than the minority hole density p (*i.e.*, $n >> p$). On illumination, let the excess electrons and holes generated be Δn and Δp, respectively:

$$n' = n + \Delta n$$

$$p' = p + \Delta p$$

Here n' and p' are the electron and hole concentrations at any particular illumination and n and p are carriers concentration when there is no illumination. Remember $\Delta n = \Delta p$ and $n >> p$. Hence, the fractional change in the majority carriers (*i.e.*, $\Delta n/n$) would be much less than that in the minority carriers (*i.e.*, $\Delta p/p$). In general, we can state that the fractional change due to the photo-effects on the *minority carrier dominated reverse bias current* is more easily measurable than the fractional change in the forward bias current. Hence, photodiodes are preferably used in the reverse bias condition for measuring light intensity.

S22. The solar radiation spectrum received by us is shown in figure.



The maxima is near 1.5 eV. For photo-excitation, $h\nu > E_g$. Hence, semiconductor with band gap ~1.5 eV or lower is likely to give better solar conversion efficiency. Silicon has $E_g \sim 1.1$ eV while for GaAs it is ~1.53 eV. In fact, GaAs is better (in spite of its higher band gap) than Si because of its relatively higher absorption coefficient. If we choose materials like CdS or CdSe ($E_g \sim 2.4$ eV), we can use only the high energy component of the solar energy for photo-conversion and a significant part of energy will be of no use.

The question arises: why we do not use material like PbS ($E_g \sim 0.4$ eV) which satisfy the condition $h\nu > E_g$ for ν maxima corresponding to the solar radiation spectra? If we do so, most of the solar radiation will be absorbed on the *top-layer* of solar cell and will not reach in or near the depletion region. For effective electron-hole separation, due to the junction field, we want the photo-generation to occur in the junction region only.

S23. Given: e.m.f. of the source,

$$E = 3.0\,\text{V}$$

Barrier potential developed in the diode,

$$V_d = 0.7\,\text{V}$$

Therefore, potential drop across the external resistance,

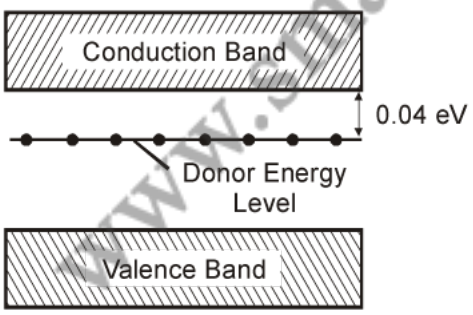
$$V = E - V_d = 3.0 - 0.7 = 2.3\,\text{V}$$

Hence, current in the circuit,

$$I = \frac{V}{R} = \frac{2.3}{100} = 2.3 \times 10^{-2}\,\text{A} = 23\,\text{mA}.$$

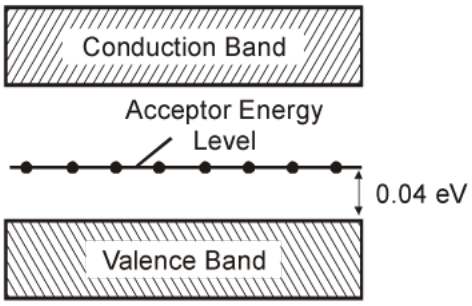
S24. When a *p-n* junction is formed, a small potential difference (fictitious battery) is set up across the depletion layer. When the junction diode is reverse biased, the polarity of the applied d.c. source aids the fictitious battery. Due to this, potential drop across the junction increases and diffusion of holes and electrons across the junction decreases. It makes the width of the depletion layer larger.

S25.



When temperature of a semiconductor is increased, a greater number of electrons are raised from valence to conduction band. It may be considered, as if the width of forbidden energy gap has decreased.

S26.



When temperature of a semiconductor is increased, a greater number of electrons are raised from valence to conduction band. It may be considered, as if the width of forbidden energy gap has decreased.

S27. Given: e.m.f. of the source,

$$E = 1.5\text{V}$$

Voltage drop across the diode,

$$V_d = 0.5\text{V}$$

Maximum power rating of the diode,

$$P = 100\,\text{mW} = 0.1\,\text{W}$$

Therefore, maximum current through the diode,

$$I = \frac{P}{V_d} = \frac{0.1}{0.5} = 0.2\,\text{A}$$

Potential drop across the resistance R,

$$V = E - V_d = 1.5 - 0.5 = 1.0\,\text{V}$$

$$\therefore \quad R = \frac{V}{I} = \frac{1.0}{0.2} = \mathbf{5\,\Omega}.$$

S28. In the circuit containing two junction diodes D_1 and D_2, the diode D_2 is forward biased and D_1 is reverse biased. Therefore, the path of appreciable current will be from positive pole of the battery to its negative pole through resistance R and junction diode D_2.

S29. Given, $E_0 = 100\,\text{V}$

$$\therefore \quad E_{\text{r.m.s.}} = \frac{100}{\sqrt{2}}\,\text{V}$$

A full-wave rectifier gives output corresponding to both the half-cycles. Therefore, r.m.s. value of voltage for a complete cycle will be the same as that over a half-cycle. Hence,

$$V_{\text{r.m.s.}} = \sqrt{(100/\sqrt{2})^2} = \frac{100}{\sqrt{2}} = \mathbf{70.7\,V}.$$

S30. It is because, saturation current during reverse bias increases linearly with the increase of the intensity of light. As such, the change in reverse current is directly proportional to the change in the intensity of light and it can be easily measured.

S31. The *p-n* function diode which emits spontaneous radiation, when forward biased, is called *photodiode*.

In case of *p-n* junction diodes made of *Ga*, *As* and *P*, the radiation emitted is in visible region.

Note: In case of *Ga*, *As* and *P*, the forbidden energy gap is 1.90 eV and the radiation emitted is of wavelength 6,500 Å.

S32. A junction diode conducts during alternate half cycles of a.c. input supply. During a half cycle of conduction, the capacitor will charge itself to peak value of the supply voltage. Therefore, voltage across the capacitor,

$$V = E_0 = E_{\text{r.m.s.}}\sqrt{2}$$

$$= 220 \times \sqrt{2} = \mathbf{311.1\ V}.$$

S33. *During forward bias*: $\Delta V = 2.4 - 2 = 0.4\,\text{V}$ and $\Delta I = 80 - 60 = 20\,\text{mA} = 0.02\,\text{A}$

$$\therefore \quad r = \frac{\Delta V}{\Delta I} = \frac{0.4}{0.02} = \mathbf{20\,\Omega}$$

During the reverse bias: $\Delta V = 0 - (-2) = 2\,\text{V}$

and $\Delta I = 0 - (-0.25) = 0.25\,\mu\text{A} = 0.25 \times 10^{-6}\,\text{A}$

$$\therefore \quad r = \frac{\Delta V}{\Delta I} = \frac{2}{0.25 \times 10^{-6}} = \mathbf{8 \times 10^6\,\Omega}.$$

S34. Circuit diagram of forward biased and reverse biased *p-n* junction diode is shown below

The width of depletion layer

(a) decreases in forward bias.

(b) increases in reverse bias.

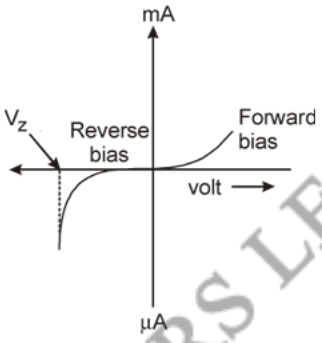
S35. With the formation of *p-n* junction, the holes from *p*-region diffuse into the *n*-region and electron-hole pair combine and get annihilated. This in turn, produces potential barrier, V_B across the junction which opposes the further diffusion through the junction. Thus, small region forms in the vicinity of the junction which is depleted of free charge carrier and has only immotile ions is called the depletion region.

S36.

S. N.	Forward bias	Reverse bias
1	Positive terminal of battery battery is connected to *p*-type and negative terminal to *n*-type Semiconductor.	Potsitive terminal of battery connected to *n*-type and negative terminal to *p*-type Semiconductor.
2.	Depletion layer is very thin.	Depletion layer is thick.
3	*p-n* junction offers very low resistance.	*p-n* junction offers very high resistance.
4	An ideal diode have zero resistance.	An ideal diode have infinite Resistance.

S37. Zener diode is used as voltage regulator.

Principle: Zener diode is operated in the reverse breakdown region. The voltage across it remain constant, equal to the breakdown voltage for large charge in reverse current.



S38. When photodiode illuminated with light due to breaking of covalent bond, equal number of additional electrons and holes comes into existence whereas fractional change in minority charge carrier is much higher than fractional change of minority carrier current is measurable significantly in reverse bias than that of forward bias. Therefore, photodiode are connected in reverse bias.

S39. Voltage drop across the series resistor,

$$V = E - V_Z = 5 - 3 = 2\,\text{V}.$$

Current through the series resistor,

$$I = \frac{V}{R} = \frac{2}{100} = 0.02\,\text{A}$$

The smallest value of the load resistance for which stabilisation occurs is that which allows a negligible (almost zero) zener current.

Therefore, current through the load resistance,

$$I_L = I = 0.02\,\text{A}.$$

Hence, smallest value of load resistance,

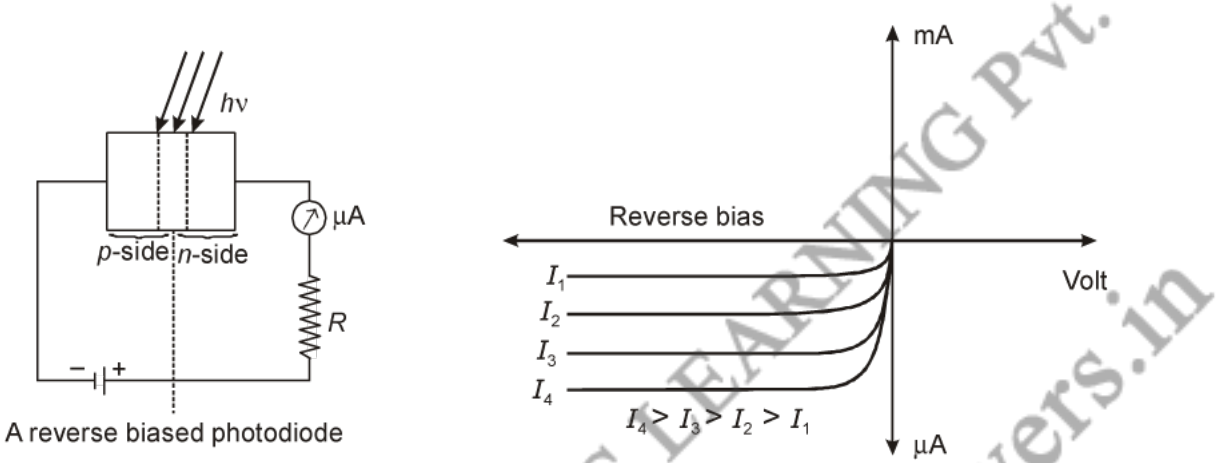
$$R_L = \frac{V_Z}{I_L} = \frac{3}{0.02} = \mathbf{150\,\Omega}.$$

S40. In Zener diode, the depletion layer width is very small (< 10^{-7} m) and hence even a very small breakdown voltage of 5 V, set up a high electric field 5×10^7 V/m which facilitating of breaking of covalent band and liberation of electrons produces large reverse current.

S41. ***Main use of photodiode:*** In demodulation of optical signal and detection of optical signal.

Main use of Zener diode: As DC voltage regulator.

S42. Circuit diagram of illuminated photodiode in reverse bias is shown below.



Hence, frequency of light ν such that $h\nu > E_g$, where E_g is band gap of increasing intensity I_1, I_2, I_3 etc., the value of reverse saturation current increases with the increase of intensity of light. Thus, the measurement of charge in the reverse saturation current can given the intensity of incident light.

S43. In a *p-n* junction diode, the expression for current is given as:

$$I = I_0 \exp\left(\frac{eV}{2k_B T} - 1\right)$$

Where, I_0 = Reverse saturation current = 5×10^{-12} A

T = Absolute temperature = 300 K

k_B = Boltzmann constant = 8.6×10^{-5} eV/K = 1.376×10^{-23} J K^{-1}

V = Voltage across the diode

(a) Forward voltage, $V = 0.6$ V

$\therefore$ Current, $$I = 5 \times 10^{-12}\left[\exp\left(\frac{1.6 \times 10^{-19} \times 0.6}{1.376 \times 10^{-23} \times 300}\right) - 1\right]$$

$$= 5 \times 10^{-12} \times \exp [22.36] = 0.0256\,\text{A}$$

Therefore, the forward current is about 0.0256 A.

(b) For forward voltage, $V' = 0.7$ V, we can write:

$$I' = 5 \times 10^{-12} \left[\exp \left(\frac{1.6 \times 10^{-19} \times 0.7}{1.376 \times 10^{-23} \times 300} - 1 \right) \right]$$

$$= 5 \times 10^{-12} \times \exp [26.25] = 1.257\,\text{A}$$

Hence, the increase in current,

$$\Delta I = I' - I$$

$$= 1.257 - 0.0256 = 1.23\,\text{A}$$

(c) $$\text{Dynamic resistance} = \frac{\text{Change in voltage}}{\text{Change in current}}$$

$$= \frac{0.7 - 0.6}{1.23} = \frac{0.1}{1.23} = 0.081\,\Omega$$

(d) If the reverse bias voltage changes from 1 V to 2 V, then the current (I) will almost remain equal to I_0 in both cases. Therefore, the dynamic resistance in the reverse bias will be infinite.

S44. A vacancy created in the covalent band of a semiconductor is called hole.

The characteristics as follows:

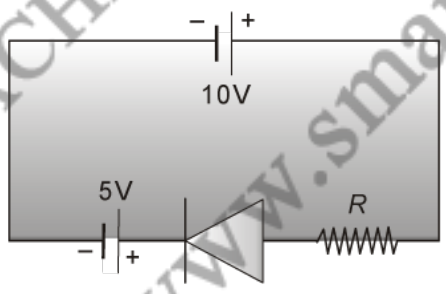
(a) A hole is equivalent to a positively charged particle having charge equal to that of an electron.

(b) Its contributes to the conductivity of semiconductor.

(c) Its energy is higher the farther below it is from the valence band.

(d) The effective mass of a hole is higher than that of an electron.

S45. The circuit shown in above figure (a) can be redrawn as shown figure below



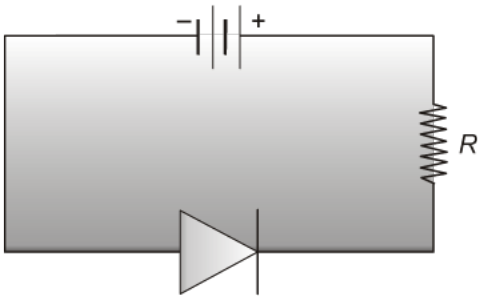
The battery of 10 V makes *p*-section at +10 V, which the battery of 5 V makes *n*-section at + 5 V. Therefore, *p*-section is at net + 5 V w.r.t. *n*-section.

Hence, the diode in the circuit shown in above figure (a) is ***forward biased***.

Similarly, by redrawing the circuit shown in the above figure (b), it can be shown that *p*-section is at net +7V w.r.t *n*-section.

Hence the diode is ***forward biased***.

S46. The circuit shown in the above figure (a) can be redrawn as shown in the figure below



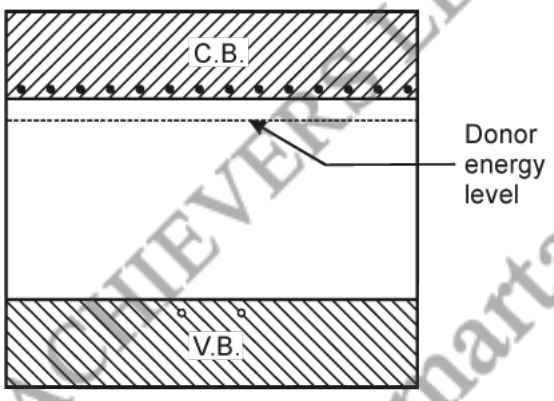
As the *p*-section is connected to negative terminal of the battery, the diode has been ***reverse biased***.

By redrawing the circuit diagrams, it can be shown the diode in circuit shown in the above figure (b) is ***reverse biased*** and in the circuit shown in the above figure (c), the diode is ***forward biased***.

S47. ***Depletion Region:*** A layer, created around the junction between *p* and *n*-section of a junction diode devoid of holes and electrons, is called ***depletion region***.

Potential Barrier: The potential difference developed across the junction due to migration of majority carriers is called ***potential barrier***.

S48. The energy band diagram of an *n*-type semiconductor is shown in figure below. Such semiconductors have a large number of free electrons (majority carriers) and a small number of holes (minority carriers). The fifth electron of donor atom is bound to it with a small energy of about 0.045 eV. Therefore, donor energy level is created just below (0.045 eV) the conduction band.



n-type semiconductor

S49. The above figure (a) shows ***forward biased*** and figure (b) shows the ***reverse biased***.

S50. (a) From $V_{be} - I_b$ characteristic at V_{cc} = 20 V [as shown in above figure], corresponding to I_{ce} = 40 μA, V_{be} = **0.7 V** and corresponding to I_b = 80 μA, V_{be} = **0.8 V**

(b) $$R(\text{at } V_{be} = 0.7\text{ V}) = \frac{0.7}{40 \times 10^{-6}} = 17{,}500\ \text{k}\Omega = \mathbf{17.5\ k\Omega}.$$

$$R(\text{at } V_{be} = 0.8\text{ V}) = \frac{0.8}{80 \times 10^{-6}} = 10{,}000\ \Omega = \mathbf{10\ k\Omega}$$

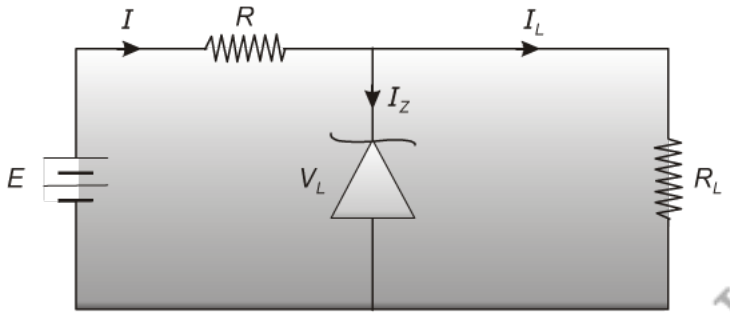
$$\text{Dynamic resistance} = \frac{\Delta V_{be}}{\Delta I_b} = \frac{0.8 - 0.7}{80 \times 10^{-6} - 40 \times 10^{-6}}$$

$$= \frac{0.1}{40 \times 10^{6}} = 2500\,\Omega = \mathbf{2.5\,k\Omega}.$$

S51. (a) The figure shows the potential drop across series resistor,

$$V = E - V_Z = 12 - 9 = 3\,\text{V}$$

$$\therefore \quad I = \frac{V}{R} = \frac{3}{200} = 0.015\,\text{A}$$



Power dissipated in the resistance R,

$$P_R = VI = 3 \times 0.015 = \mathbf{0.045\,W}$$

(b) Current through R_L,

$$I_L = \frac{9}{1.5 \times 10^{3}} = 0.006\,\text{A}$$

Power dissipated in R_L,

$$P_L = V_Z I_L = 9 \times 0.006 = \mathbf{0.054\,W}$$

(c) Current through the zener diode,

$$I_Z = I - I_L = 0.015 - 0.06 = 0.009\,\text{A}$$

Power dissipated in the zener diode,

$$P_Z = V_Z I_Z = 9 \times 0.009 = \mathbf{0.081\,W}.$$

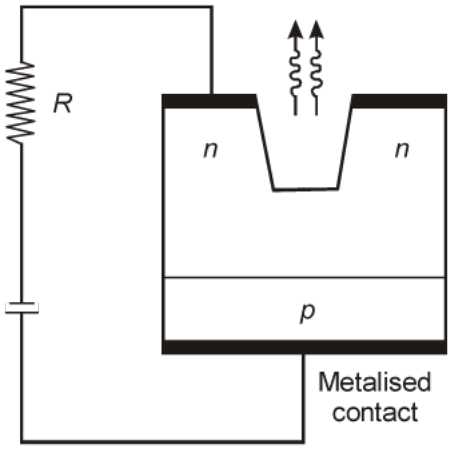
S52. **Application:** LEDs are used in remote controls, burglar alarms, watches, calculators, computers, etc. However, they are found to be of great use in optical communication.

When voltage is applied to the LED, electrons move across the junction into the *p*-region. Each time an electron recombines with a positive hole, electric potential energy is converted into electromagnetic energy and a photon of light with a frequency characteristic of the semiconductor material is emitted. In GaAsP, the forbidden energy gap is 1.97 eV. The wavelength of radiation emitted is given by

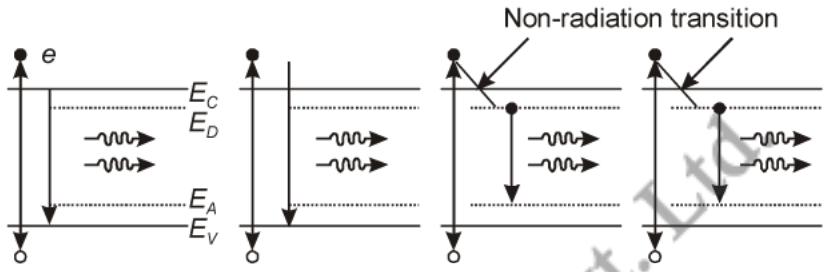
$$\lambda = \frac{hc}{E_g} = \frac{6.62 \times 10^{-34} \times 3 \times 10^{8}}{1.97 \times 1.6 \times 10^{-19}} = 6.30 \text{ nm.}$$

This wavelength lies in the visible region. Thus, for the fabrication of visible light LEDs, the forbidden energy gap should be of about 1.8 eV.

S53. **A light emitting diode (LED)** is a *p-n* junction diode emit spontaneous radiation in visible range due to recombination of electron and holes. Its circuit diagram is shown in figure (a). It is connected in forward bias mode through a resistance R to limit the current through it.



(a) A typical LED



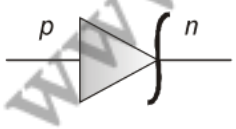
(b) Different transitions giving luminescence

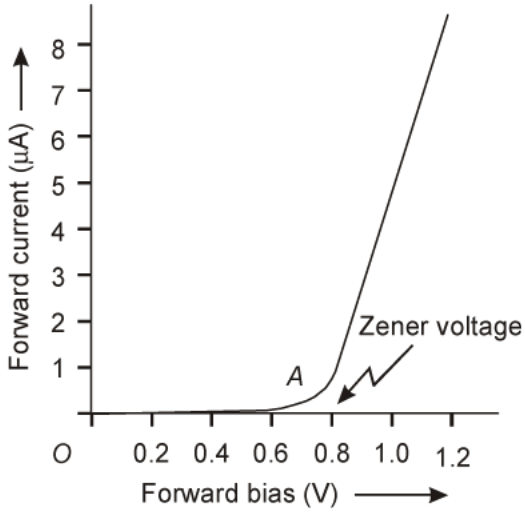
Working: The mechanism of spontaneous emission of light can be understood with help of figure (b). In a semiconduction besides conductor and valence bands, there are donor level (near conduction band) and acceptor level (near valence band). When electron from conduction and donor level makes transition to valence or acceptor level containing holes, the energy in the form of light radiation is released.

The semiconducting material used in LED is chosen according to colour or wavelength of light radiation. LEDs for red, green and orange are available. The energy gap E_g for LED should be between 2.8 eV to 1.8 eV (as visible radiations lie in the range 4500 nm to 7000 nm). Thus the least band gap of the material should be 1.8 eV. Naturally, Si ($E_g \approx 1.1$ eV) and Ge (E_g 0.7 eV) are not suitable due to low value (<1.8 eV) of energy band gap. Phosphorus doped GaAs ($GaAs_{1-x}P_x$) and GaP are widely used materials for LEDs.

S54. A zener diode is used as a voltage regulator.

Symbol:





S55. (a) Photodiode is connected in reverse bias and feeble reverse current flows due to thermally generated electron-hole pair, known as dark current. When light of suitable frequency (ν) such that $h\nu > E_g$, where E_g is band gap is incident on diode, additional electron - hole pair generated and current flows in the circuit.

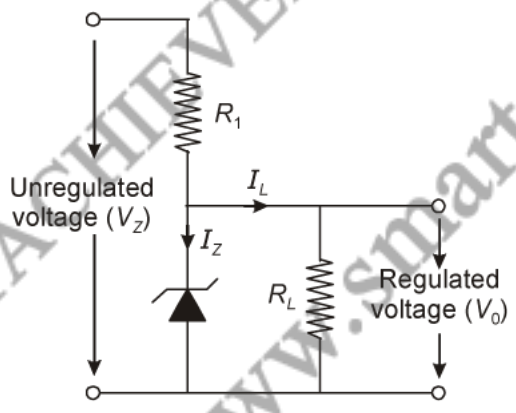
(b) So that majority carriers from the emitter region cross over to the collector with least recombination's in the base region.

(c) Base current is reduced due to higher recombination in the base region.

S56. ***Zener diode fabrication:*** Zener diode is made by heavily doping both *p* and *n*-type semiconductors and hence the width of depletion layer becomes thin which lead to produce large electric field to increase the current even on applying reverse voltage of 4 or 5 V.

Zener diode is used as voltage regulator.

These electrons are responsible for the high current at the breakdown.



Voltage regulator converts an unregulated DC output of rectifier into a constant regulated DC voltage, using Zener diode. The unregulated voltage is connected to the Zener diode through a series resistance R_1 such that the Zener diode is reverse biased. If the input voltage inreases, the current through R_1 and Zener diode increases. Thus, the voltage drop across R_1 increases without any change in the voltage drop across Zener diode. This is because of the breakdown region, Zener voltage remain constant even though the current through Zener diode changes.

Similarly, if the input voltage decreases, the current through R_1 and Zener diode decreases. The voltage drop across R_1, decreases without any change in the voltage across the Zener diode.

Now, any change in input voltage results the change in voltage drop across R_1, without any change in voltage across the Zener diode.

Thus, Zener diode acts as a voltage regulator.

S57. Given: $E_{\text{r.m.s.}} = 30\,\text{V}$

Therefore, peak value of supply voltage.

$$E_0 = E_{\text{r.m.s.}} \times \sqrt{2} = 30\sqrt{2}\,\text{V}$$

(a) Since the forward resistance of diode is negligible, peak value of current through R_L,

$$I_0 = \frac{E_0}{R_L} = \frac{30\sqrt{2}}{10 \times 10^3} = 3\sqrt{2} \times 10^{-3}\,\text{A} = \mathbf{4.24\ mA}$$

(b) The d.c. milliameter connected in series to load resistance R_L measures the average value of current over the complete cycle. Therefore,

$$\text{Reading of d.c. milliameter} = \frac{(2I_0/\pi) + 0}{2} = \frac{I_0}{\pi} = \frac{4.24}{\pi} = 1.35\ \text{mA}$$

(c) When a capacitor is connected across R_L, the capacitor charges to peak supply and when diode is not conducting it discharges through R_L.

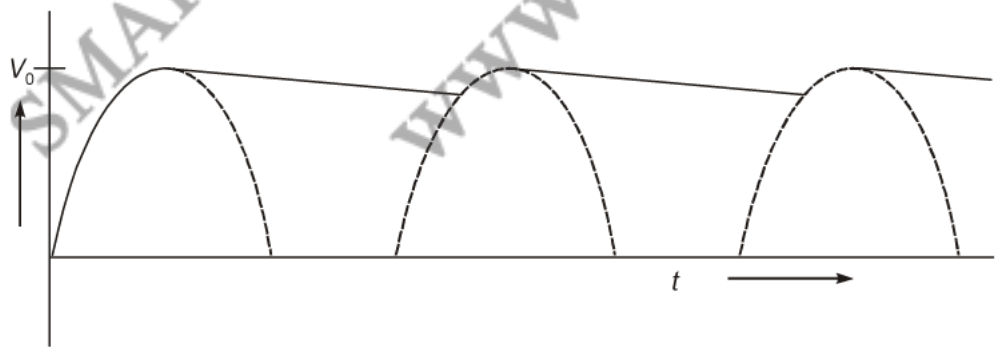
Now, time period of supply voltage,

$$T = \frac{1}{f} = \frac{1}{50} = \mathbf{0.02\ s}$$

Time constant of *CR*-circuit,

$$CR = 16 \times 10^{-6} \times 10 \times 10^3 = \mathbf{0.16\ s}$$

Since $CR >> T$, the output voltage across capacitor will practically remain equal to the peak value of supply voltage and hence output will be as shown in figure given below



Hence, reading of d.c. voltmeter connected across C

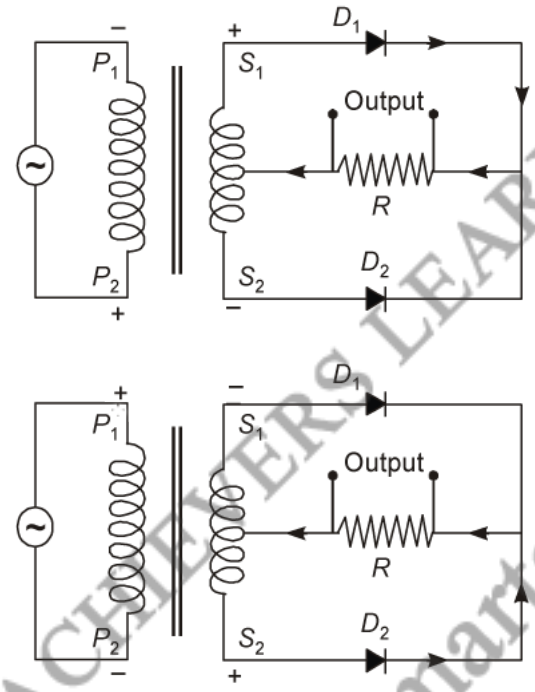
$$= 20\sqrt{2}\ \text{V}\ .$$

S58. ***Full-wave rectifier:*** The circuit diagram of a full-wave rectifier is shown in figure. The a.c. to be rectified is fed to the primary terminals of a centre-tapped transformer.

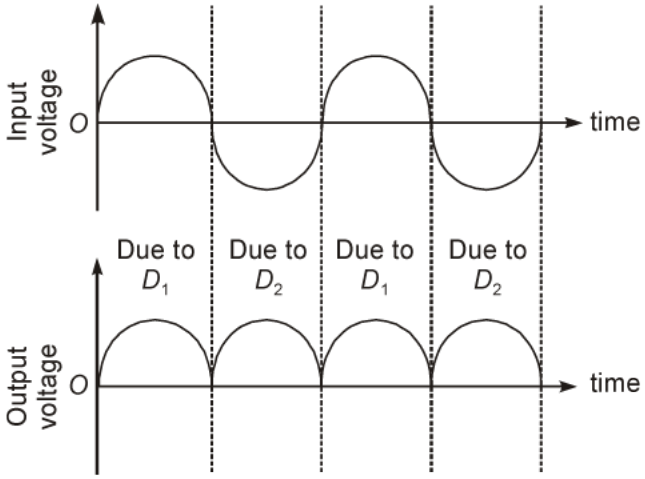
During the first (positive) half cycle of the a.c. input, the upper end of the secondary coil acquires positive potential and the lower end acquires negative potential. As a result, diode D_1 gets forward biased and diode D_2 gets reverse biased. Diode D_1 conducts and a current flows through load, as shown by continuous in Figure.

During the next (negative) half cycle of the a.c. input, the upper end of the secondary coil acquires negative potential and the lower end acquires positive potential. As a result, diode D_1 gets reverse biased and diode D_2 gets forward biased. Diode D_2 conducts and a current flows through load, as shown by dotted lines in figure. The direction of current remains same as in the previous half cycle.

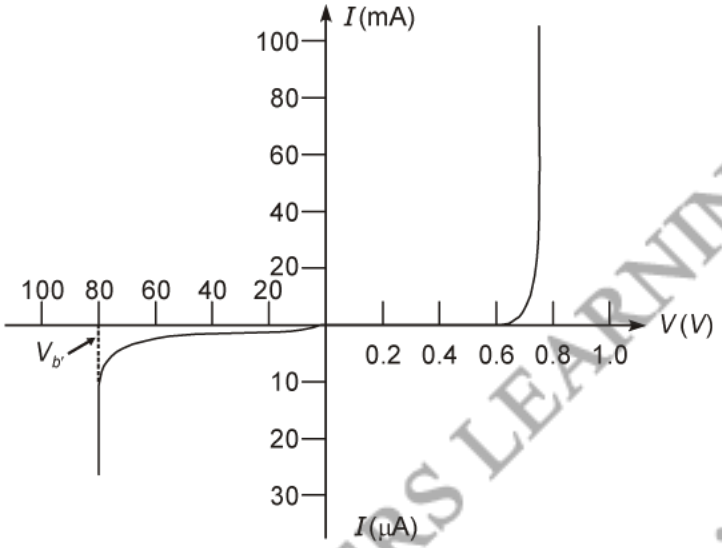
The circuit diagram of full wave rectifier is shown below.



The input and output waveforms have been given below.



S59. *V-I* characteristics of *p-n* junction diode.

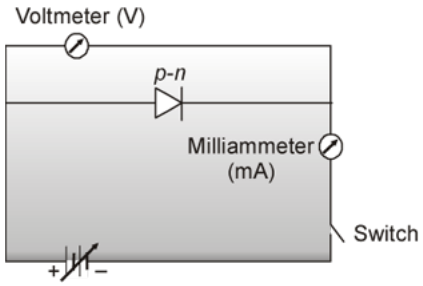


(a) Under the reverse bias condition, the holes of *p*-side are attracted towards the negative terminal of the battery and the electrons of the *n*-side are attracted towards the positive terminal of the battery. This increases the depletion layer and the potential barrier. However the minority charge carriers are drifted across the junction producing a small current. At any temperature, the number of minority carriers is constant so there is the small current at any applied potential. This is the reason for the current under reverse bias to be almost independent of applied potential. At the critical voltage, avalanche breakdown takes place which results in a sudden flow of large current.

(b) At the critical voltage, the holes in the *n*-side and conduction electrons in the *p*-side and conduction electrons in the *p*-side are accelerated due to the reverse-bias voltage. These minority carriers acquire sufficient kinetic energy from the electric field and collide with a valence electron. Thus the bond is finally broken and the valence electrons move into the conduction band resulting in enormous flow of electrons and thus formation of hole-electron pairs. Thus there is a sudden increase in the current at the critical voltage.

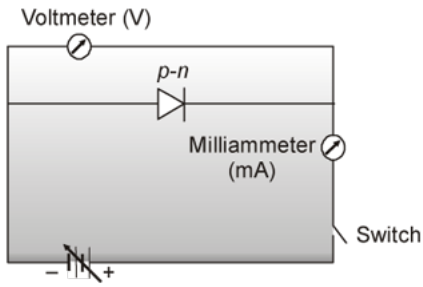
Zener diode is a semiconductor device which operates under the reverse bias in the breakdown region.

S60. (a) (i)



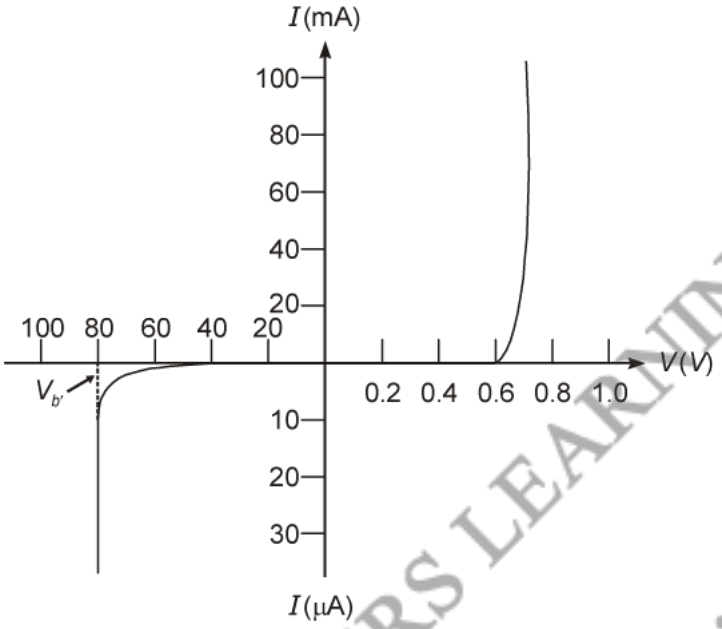
forward bias

(ii)



reversed bias

The battery is connected to the silicon diode through a potentiometer (or rheostat), so that the applied voltage can be changed. For different values of voltages, the value of current is noted.



(b) Light emitting diode (LED) is a heavily doped *p-n* junction which under forward bias emits spontaneous radiations.

Two important LEDs advantages:

(i) Low operational voltage and less power

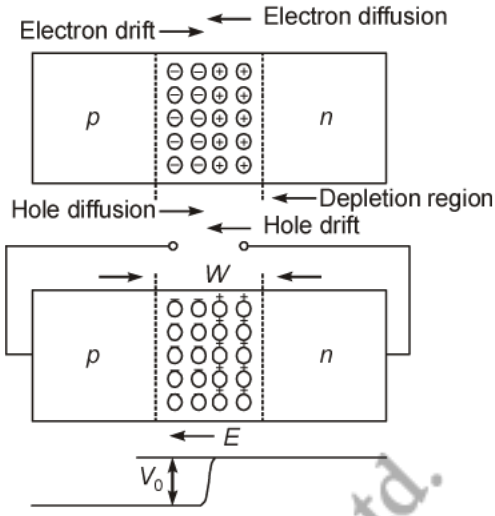
(ii) Fast on-off switching capability.

S61. (a) Two important processes involved in the formation of *p-n* junction are:

(i) diffusion (ii) drift

During the formation of *p*-*n* junction due to concentration gradient there is movement of electrons and holes across the function from higher concentration to lower concentration side, Holes diffuse from *p*-side to *n*-side and electrons diffuse from *n*-side to *p*-side. This motion of charges develops diffusion current.

When electrons diffuse from *n*- to *p*-side they leave behind positively charged ionised donor on *n*-side. A layer of positive charge is developed. Similarly, when hole diffuses from *p*- to *n*-side they leave behind negatively charged ionised acceptor atoms. As a result a layer of negative charge is developed on the *p*-side.

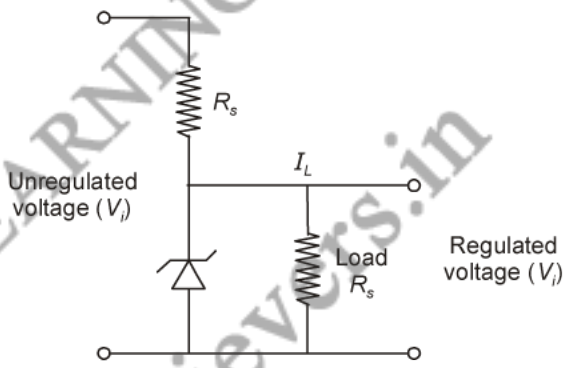


Motion of charge carriers due to electric field is called drift. It is in opposite direction w.r.t. the diffusion current.

With time diffusion current decreases and drift current increases. The process of diffusion continues till diffusion current equals the drift current. At this moment the *p*-*n* junction is formed. We say *p*-*n* junction is under equilibrium and there is no current.

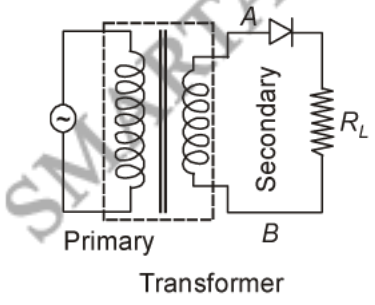
(b) Zener diode is used as a voltage regulator.

Unregulated d.c. voltage is supplied to the circuit. Increase in input voltage increases current through R_s and zener diode. Voltage drop across R_s increases but across zener diode remains same because in the breakdown region, zener voltage remains constant for a large variation of current through the zener diode similarly for a decrease in voltage, there is a decrease in potential drop across R_s but no change across the zener diode. This way voltage is regulated.

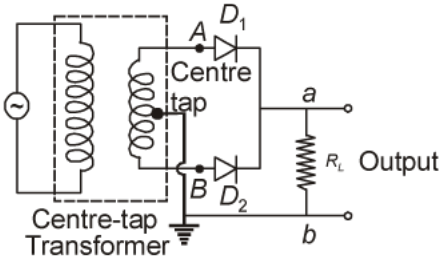


S62. (a) X is half wave rectifier.

Y is full wave rectifier.

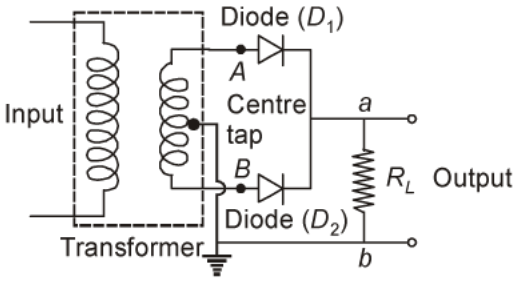


Half wave rectifier



Full wave rectifier

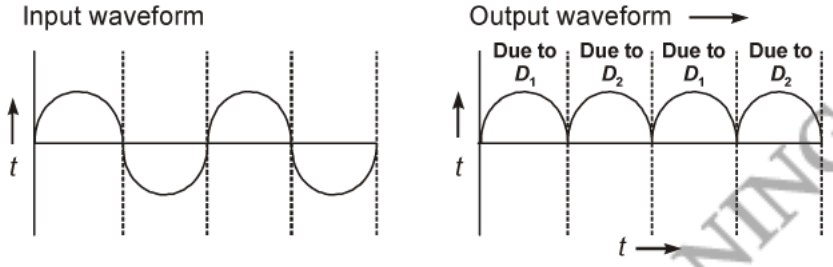
(b) Circuit



Working Principal: "Diode conducts only in forward bias". Suppose

(i) During + ve half of the input cycle diode D_2 is in forward biased and conducts, through the load resistance from *a* to *b* side.

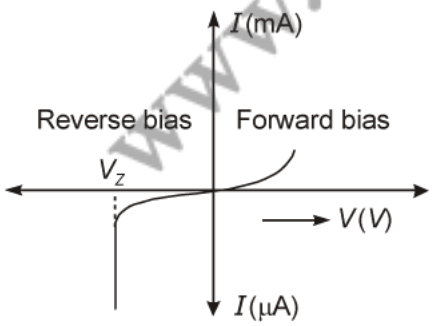
(ii) During – ve half of the input cycle diode D_1 is under forward biasing and conducts, again through the load resistance from *a* to *b* side.



(c) When voltage across capacitor increases it gets charge. When voltage decreases capacitor looses charge. This way capacitor maintains voltages and filters out a.c. component and gives d.c. voltage.

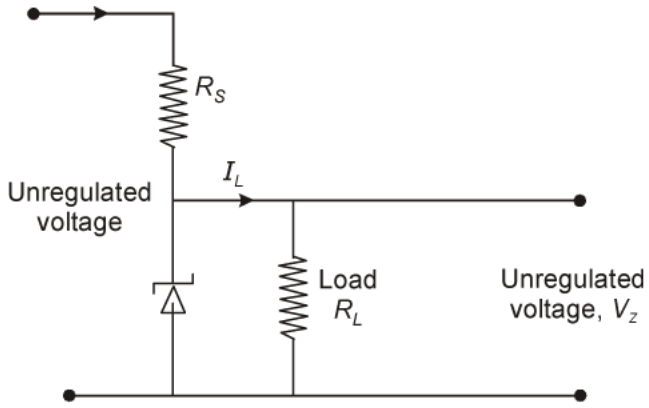
S63. Zener diode works only in reverse breakdown region that is why it is considered as a special purpose semiconductor.

I-V characteristics of Zener diode, is given below.



Reverse current is due to the flow of electrons from $n \rightarrow p$ and holes from $p \rightarrow n$. As the reverse biased voltage increase the electric field across the junction, increases significantly and when reverse bias voltage $V = V_Z$, then the electric field strength is high enough to pull the electrons from p-side and accelerated it to *n*-side.

These electrons are responsible for the high current at the breakdown.



Voltage regulator converts an unregulated DC output of rectifier into a constant regulated DC voltage, using Zener diode. The unregulated voltage is connected to the Zener diode through a series resistance R_S such that the Zener diode is reverse biased. If the input voltage increases, the current through R_S and Zener diode increases. Thus, the voltage drop across R_S increases without any change in the voltage drop across Zener diode. This is because of the breakdown region, Zener voltage remain constant even though the current through Zener diode changes.

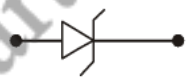
Similarly, if the input voltage decreases, the current through R_S and Zener diode decreases. The voltage drop across R_S, decreases without any change in the voltage across the Zener diode.

Now, any change in input voltage results the change in voltage drop across R_S, without any change in voltage across the Zener diode.

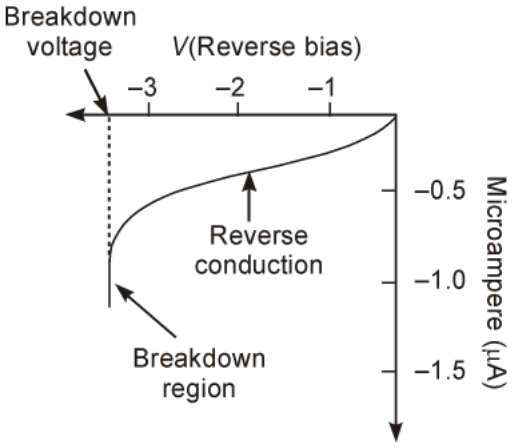
Thus, Zener diode acts as a voltage regulator.

S64. (a) Device, *D* is a Zener diode.

Symbol of Zener diode

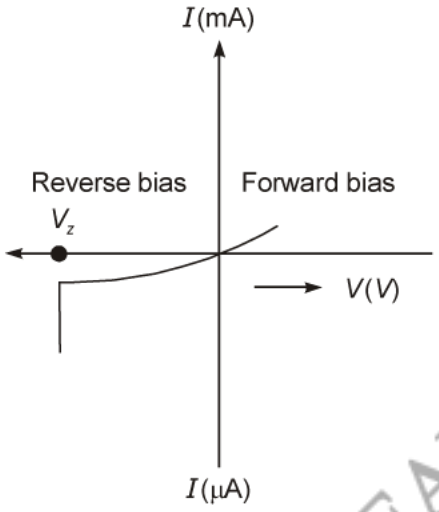


(b) In forward bias, junction diode does not obey Ohm's law. Initially current increases slowly till cut-in voltage, Knee voltage or threshold voltage, V_K for threshold voltage, V_K (for *Si*, $V_K = 0.7$ V). After V_K, diode current increases linearly (and abruptly). In reverse bias, a very feeble current flows due to drift current because of minority charge carrier. When the reverse bias reaches to sufficient large value, the reverse current increases suddenly to a large value. This voltage is referred as breakdown voltage.

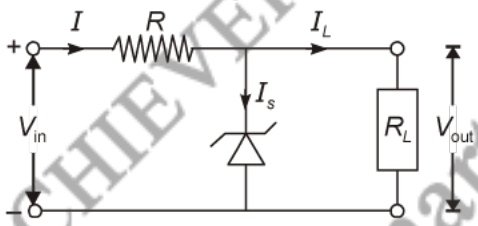


Reverse characteristic of junction diode

S65. (a) ***V – I* characteristics of a Zener diode:**



(b) **Use of a Zener diode as a voltage regulator:** Voltage regulation is a measure of a circuit's ability to maintain a constant output voltage even when either input voltage or load current varies.



A zener diode when working in the breakdown region can serve as a voltage regulator. In the figure, V_{in} is the input d.c. voltage whose variations are to be regulated. The zener diode is reverse connected-across V_{in}. When potential difference across the diode is greater that V, it conducts and draws relatively large current through the series resistance R. The load resistance R_L across which a constant voltage V_{out} is required, is connected in parallel with the diode. The total current I passing through R equals the sum of diode current and load current.

i.e., $I = I_d + I_L$

It will be seen under all conditions

$$V_{out} = V_z$$

Hence, $$V_{in} = I_R + V_{out}$$

$$V_{in} = I_R + V_z.$$

(c) Consider, say, the care of *n*-type semiconductor. On illumination excess holes and electrons generated would be Δp and Δn.

$$n' = n + \Delta n$$

$$p' = p + \Delta p$$

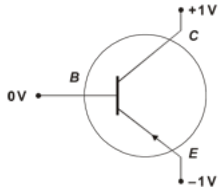
Here, $$\Delta n = \Delta p$$

$$n >> p.$$

So we find that fractional change in the majority carriers ($\Delta n / n$) would be much less than that in the minority carriers ($\Delta p / p$). As change in reverse saturation current is more pronounced that current in forward biased, photodiodes are used in reverse bias.

Date: 22/10/2021

Q1. In the figure below, is (a) the emitter and the (b) collector forward or reverse biased?



Q2. For a transistor amplifier, the voltage gain

(a) remains constant for all frequencies.

(b) is high at high and low frequencies and constant in the middle frequency range.

(c) is low at high and low frequencies and constant at mid frequencies.

(d) None of the above.

Q3. For transistor action, which of the following statements are correct:

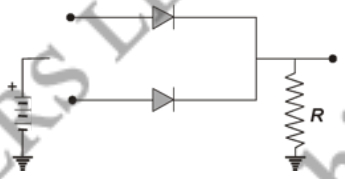
(a) Base, emitter and collector regions should have similar size and doping concentrations.

(b) The base region must be very thin and lightly doped.

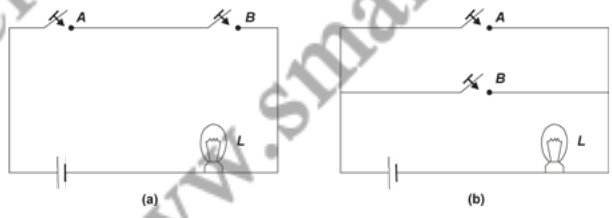
(c) The emitter junction is forward biased and collector junction is reverse biased.

(d) Both the emitter junction as well as the collector junction are forward biased.

Q4. Name the logic gate realised using *p-n* junction diodes as shown in figure below. Give its logic symbol.



Q5. In the circuits shown, a switch which is opened represents the logic state 0 and the switch which is closed represents the logic state 1. The lamp *L* is lit, when output is logic state 1. What types of gates are represented by the circuits shown in figure below (a) and (b).



Q6. Define the transconductance of a transistor.

Q7. Write the relation between current gains α and β.

Q8. Define current amplification factor in a common emitter mode of transistor.

Q9. Define input resistance of a transistor used in its common emitter configuration.

Q10. In *p-n-p* transistor, what are the current carriers inside and outside the transistor circuit?

Q11. In *n-p-n* transistor, what are the current carriers inside and outside the transistor circuit?

Q12. The truth table of a logic gate has the form given in table below. Name this gate and draw its symbol.

A	B	*y*
0	0	1
1	0	0
0	1	0
1	1	0

Q13. Write down the truth table for a *NAND gate*.

Q14. A given logic inverts the input applied to it. Name this gate and give its symbol.

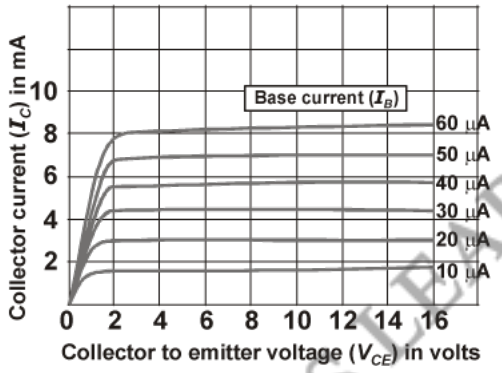
Q15. Write the truth table for an *AND gate*.

Q16. Draw the logic symbol of *AND gate*.

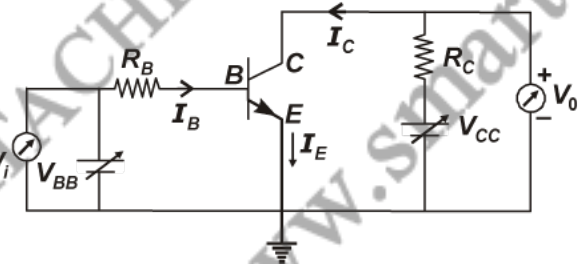
Q17. In a transistor, emitter is always forward biased. Why?

Q18. Two amplifiers are connected one after the other in series (cascaded). The first amplifier has a voltage gain of 10 and the second has a voltage gain of 20. If the input signal is 0.01 volt, calculate the output ac signal.

Q19. From the output characteristics shown in figure, calculate the values of $\beta_{a.c.}$ and $\beta_{d.c.}$ of the transistor when V_{CE} is 10 V and I_C = 4.0 mA.



Q20. In figure, the V_{BB} supply can be varied from 0V to 5.0 V. The Si transistor has $\beta_{d.c.}$ = 250 and R_B = 100 kΩ, R_C = 1 KΩ, V_{CC} = 5.0V. Assume that when the transistor is saturated, V_{CE} = 0V and V_{BE} = 0.8 V. Calculate (a) the minimum base current, for which the transistor will reach saturation. Hence, (b) determine V_1 when the transistor is 'switched on'. (c) find the ranges of V_1 for which the transistor is 'switched off' and 'switched on'.



Q21. For a CE transistor amplifier, the audio signal voltage across the collector resistance of 2.0 kΩ is 2.0 V. Suppose the current amplification factor of the transistor is 100, What should be the value of R_B in series with V_{BB} supply of 2.0 V if the d.c. base current has to be 10 times the signal current. Also calculate the dc drop across the collector resistance.

Q22. The a.c. current gain of a common emitter amplifier is 20. If input and output resistances are 2 kΩ and 5 kΩ respectively, find (a) voltage gain and (b) power gain.

Q23. Define current gains, α and β of a transistor.

Q24. Why the output voltage is out of phase with the input voltage in a common emitter transistor amplifier?

Q25. In a transistor, emitter base junction is always forward-biased, while the collector-base junction is reverse biased. Why?

Q26. Why a transistor cannot be used as a rectifier?

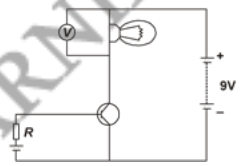
Q27. In a transistor, doping level in base is increased slightly. How will it affect (a) collector current and (b) base current?

Q28. The input resistance of a transistor is 1,000 Ω. On changing its base current by 10 μA, the collector current increases by 2 mA. If a load resistance of 5 kΩ is used in the circuit, calculate (a) the current gain and (b) voltage gain of the amplifier.

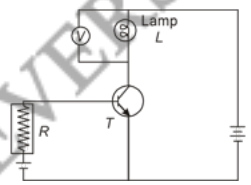
Q29. For a transistor working as common base amplifier, current gain is 0.96. If the emitter current is 7.2 mA, calculate the base current.

Q30. A change of 8.0 mA in the emitter current causes a change of 7.9 mA in the collector current. How much change in base current is required to have the same change of 7.9 mA in the collector current? Find the values of α and β.

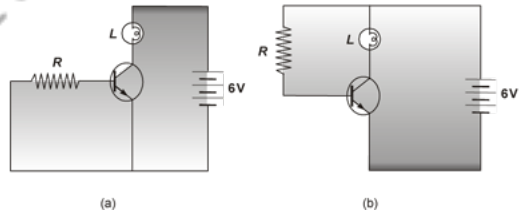
Q31. In the given circuit diagram a voltmeter V is connected across a lamp *L*. How would the brightness of the lamp and voltmeter reading *V* be affected, if the value of resistance *R* is decreased? justify your answer.



Q32. In the given circuit, a voltmeter, *V* is connected across lamp, *L*. What changes would you observe in the lamp, *L* and the voltmeter, if the value of resistor *R* is reduced?



Q33. In only one of the circuits given below, the lamp *L* lights. Which circuit is it? Give reason for your answer.



Q34. The input resistance of a silicon transistor is 665 Ω. Its base current is changed by 15 μA, which results in the change in collector current by 2 mA. This transistor is used as a common emitter amplifier with a load resistance of 5 kΩ. Calculate (a) current gain $\beta_{a.c.}$ (b) transconductance g_m (c) voltage gain A_v of the amplifier.

Q35. In a silicon transistor, the base current is changed by 20 μA. This results in a change of 0.02 V in base to emitter voltage and a change of 2 mA in the collector current.

(a) Find the input resistance, β_{ac} and transconductance of the transistor.

(b) This transistor is used as an amplifier with the load resistance 5 kΩ. What is the voltage gain of the amplifier?

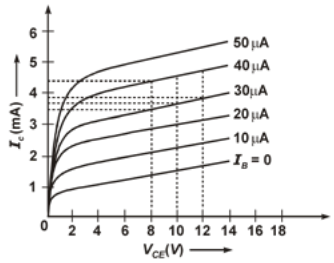
Q36. For a *CE*-transistor amplifier, the audio signal voltage across the collected resistance of 2 kΩ is 2 V. Suppose the current amplification factor of the transistor is 100, find the input signal voltage and base current, if the base resistance is 1 kΩ.

Q37. Output characteristics of an *n-p-n* transistor in *CE* configuration is shown in the figure.
Determine.

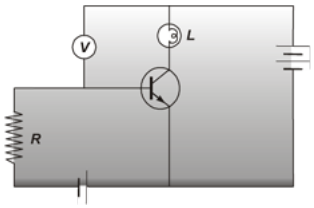
(a) dynamic output resistance

(b) *DC* current gain and

(c) *AC* current gain at an operating point V_{CE} = 10 V, when I_B = 30 μA.

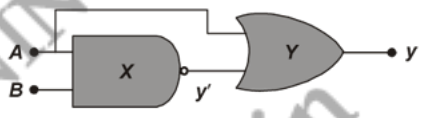


Q38. In the circuit shown in figure, a voltmeter *V* is connected across lamp *L*. What changes would occur at lamp *L* and the voltmeter *V*, if the resistor *R* is reduced in value? Give reason for your answer.



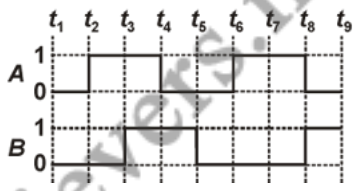
Q39. How does the collector current change in a junction transistor, if the base region has larger width?

Q40. Identify the logic gates marked *X*, *Y* in the figure below
Write down the output at *y*, when
A = 0, *B* = 1 and *A* = 1, *B* = 0.

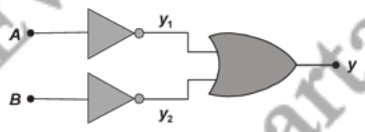


Q41. (a) Sketch the output waveform for an AND gate for the inputs *A* and *B* shown in the figure:

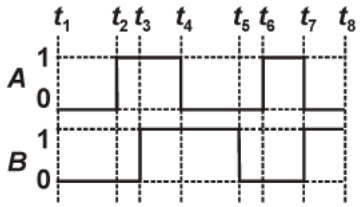
(b) If the output of above AND gate is fed to a NOT gate, name the gate of the combination is formed.



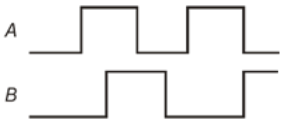
Q42. Express by a truth table, the output *y* for all possible inputs *A* and *B* for the combination of gates shown in the figure below. Hence, show that it behaves as a NAND gate.



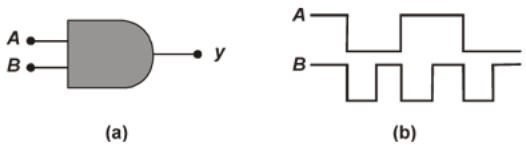
Q43. Show the output waveforms (*y*) for the inputs *A* and *B* in shown in figure below, for (a) OR gate and (b) NAND gate.



Q44. Give the logic symbol for an OR gate. Draw the output waveform for input wave forms *A* and *B* shown in the figure below, for this gate.



Q45. In the figure (a) and (b), circuit symbol of a logic gate and two input waveforms *A* and *B* are shown.



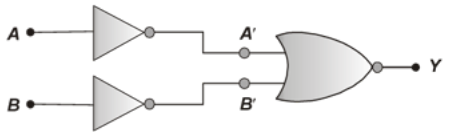
(a) (b)

Name the logic gate, write its truth table and give the output wave form.

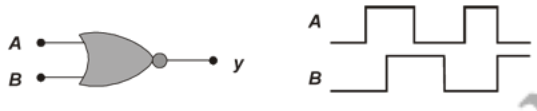
Q46. Draw a simple circuit of a *CE* transistor amplifier. Explain its working. Show that the voltage gain, A_V of the amplifier is given by $A_V = \frac{\beta_{ac} R_L}{r_i}$, where β_{ac} is the current gain, R_L is the load resistance and r_i is the input resistance of the transistor. That is the significance of the negative sign in the expression for the voltage gain?

Q47. (a) Explain briefly the principle on which a transistor-amplifier works as an oscillator. Draw the necessary circuit diagram and explain its working.

(b) Identify the equivalent gate for the following circuit and write its truth table.



Q48. In the below figure (a) and (b), circuit symbol of a logic gate and two input waveforms *A* and *B* are shown. Name the logic gate, write its truth table and give the output waveform.



(a) (b)

Q49. An XOR gate has following truth table

A	*B*	*y*
0	0	0
0	1	1
1	0	1
1	1	0

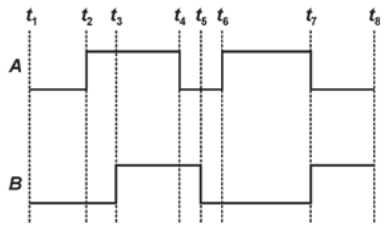
It is represented by following logic relation

$$Y = \overline{A} . B + A . \overline{B}$$

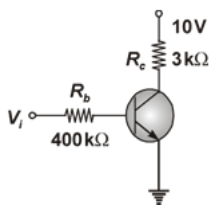
Build this gate using AND, OR and NOT gates.

Q50. (a) Draw the circuit diagram of a full wave rectifier using *p-n* junction diode. Explain its working and show the output, input waveforms.

(b) Show the output waveforms (*Y*) for the following inputs *A* and *B* of (i) OR gate (ii) NAND gate



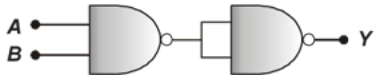
Q51. In the circuit shown here, when the input voltage of the base resistance is 10 V, V_{be} is zero and V_{ce} is also zero. Find the values of I_b, I_c and β.



Q52. (a) Explain the formation of depletion layer and potential barrier in a *p-n* junction.

(b) In the figure given below the input waveform is converted into the output waveform by a device '*X*'. Name the device and draw its circuit diagram.

(c) Identify the logic gate represented by the circuit as shown and write its truth table.



Q53. (a) Draw the circuit for studying the input and output characteristics of an *n-p-n* transistor in *CE* configuration. Show, how, from the output characteristics, the information about the current amplification factor (β_{ac}) can be obtained.

(b) Draw a plot of the transfer characteristic (V_0 versus V_i) for a base-biased transistor in *CE* configuration. Show for which regions in the plot, the transistor can operate as a switch.

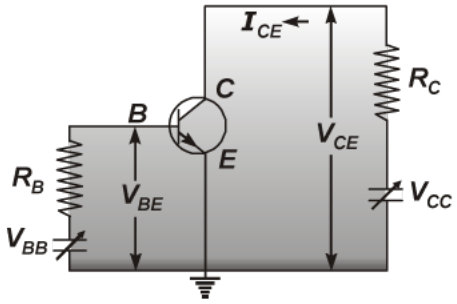
Q54. (a) Draw a circuit diagram to study the input and output characteristics of an *n-p-n* transistor in its common emitter configuration. Draw the typical input and out characteristics.

(b) Explain, with the help of a circuit diagram, the working of *n-p-n* transistor as a common emitter amplifier.

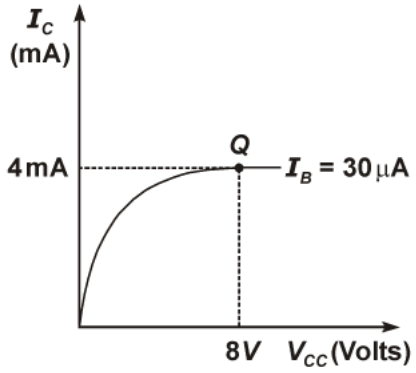
Q55. (a) Draw the circuit for studying the input and output characteristics of a transistor in *CE* configuration. Show, how from the output characteristics, the information about the current amplification factor (β_{AC}) can obtained.

(b) Draw a plot of the transfer characteristics (V_O versus V_i) for a base-biased transistor in *CE* configuration. Show for which regions in the plot, the transistor can operate as a switch.

Q56. Consider the circuit arrangement shown in the figure for studying input and output characteristics of *n-p-n* transistor in *CE* configuration.



Select the values of R_B and R_C for a transistor whose V_{BE} = 0.7 V, so that the transistor is operating at point *Q* as shown in the characteristics given in the figure.



Given that the input impedance of the transistor is very small and V_{CC} = V_{BB} = 16 V, also find the voltage gain and power gain of circuit making appropriate assumptions.

Q57. Explain the function of base region of a transistor. Why is this region made thin and lightly doped?

Draw a circuit diagram to study the input and output characteristics of *n-p-n* transistor in a common emitter (*CE*) configuration. Show these characteristics graphically. Explain how current amplification factor of the transistor is calculated using output characteristics.

Date: 22/10/2021

S1. Of the *p-n-p* transistor shown in above figure

(a) As the emitter is negative w.r.t. base, it is *reverse biased* and

(b) As the collector is positive w.r.t base, is is *forward biased*.

S2. The correct statement is **(c)**.

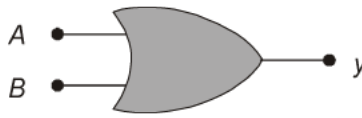
The voltage gain of a transistor amplifier is constant at mid frequency range only. It is low at high and low frequencies.

S3. The correct statement is **(b)**, **(c)**.

For a transistor action, the junction must be lightly doped so that the base region is very thin. Also, the emitter junction must be forward-biased and collector junction should be reverse-biased.

S4. It is *OR gate*.

For logic symbol of *OR gate*, (see figure below).



S5. (a) AND gate (b) OR gate.

S6. It is defined as the ratio of change in collector current to the change in base-emitter voltage.

It is denoted by g_m.

Mathematically, $g_m = \frac{\Delta I_c}{\Delta V_{be}}$.

S7. $\beta = \frac{\alpha}{1-\alpha}$.

S8. It is defined as the ratio of change in collector current to the change in base current at constant collector voltage.

It is denoted by β.

Mathematically, $\beta = \left(\frac{\Delta I_c}{\Delta I_b}\right)_{V_{ce}}$.

S9. It is defined as the ratio of small change in base voltage to the small change produced in base current at constant collector voltage.

It is denoted by R_{in}.

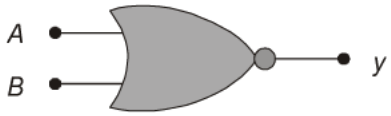
Mathematically, $R_{in} = \left(\frac{\Delta V_{be}}{\Delta I_b}\right)_{V_{ce}}$.

S10. Holes are the current carriers through the transistor but the electrons in the external circuit.

S11. Electrons are the current carriers through the transistor and holes in the external circuit.

S12. It is a *NOR gate*.

For its symbol, (see figure below).

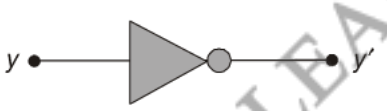


S13.

A	B	*y*
0	0	1
1	0	1
0	1	1
1	1	0

S14. It is a *NOT gate*.

For its symbol, (see figure below).



S15.

A	B	*y*
0	0	0
1	0	0
0	1	0
1	1	1

S16.

S17. The emitter is always forward biased to enable the majority carriers to cross the emitter base junction, so that current flows through the transistor.

S18. Voltage gain of the first amplifier, $V_1 = 10$

Voltage gain of the second amplifier, $V_2 = 20$

Input signal voltage, $V_i = 0.01\,V$

Output A.C. signal voltage $= V_0$

The total voltage gain of a two-stage cascaded amplifier is given by the product of voltage gains of both the stages, *i.e.*,

$$V = V_1 \times V_2$$
$$= 10 \times 20 = 200$$

We have the relation: $V_2 = 20$

$$V_0 = V \times V_i$$
$$= 200 \times 0.01 = 2\,\text{V}$$

Therefore, the output A.C. signal of the given amplifier is 2 V.

S19.

$$\beta_{\text{a.c.}} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}, \qquad \beta_{\text{d.c.}} = \frac{I_C}{I_B}$$

For determining $\beta_{\text{a.c.}}$ and $\beta_{\text{d.c.}}$ at the stated values of V_{CE} and I_C one can proceed as follows. Consider any two characteristics for two values of I_B which lie above and below the given value of I_C. Here I_C = 4.0 mA. (Choose characteristics for I_B = 30 and 20 μA.) At V_{CE} = 10 V we read the two values of I_C from the graph. Then

$$\Delta I_B = (30 - 20)\,\mu\text{A} = 10\,\mu\text{A},\ \Delta I_C$$
$$= (4.5 - 3.0)\,\text{mA} = 1.5\,\text{mA}$$

Therefore, $\beta_{\text{a.c.}} = 1.5\,\text{mA}/10\,\mu\text{A} = 150$

For determining $\beta_{\text{d.c.}}$, either estimate the value of I_B corresponding to I_C = 4.0 mA at V_{CE} = 10 V or calculate the two values of $\beta_{\text{d.c.}}$ for the two characteristics chosen and find their mean.

Therefore, for $I_C = 4.5\,\text{mA}$ and $I_B = 30\,\mu\text{A}$,

$$\beta_{\text{d.c.}} = 4.5\,\text{mA}/30\,\mu\text{A} = 150$$

and for $I_C = 3.0\,\text{mA}$ and $I_B = 20\,\mu\text{A}$

$$\beta_{\text{d.c.}} = 3.0\,\text{mA}/20\,\mu\text{A} = 150$$

Hence, $\beta_{\text{d.c.}} = (150 + 150)/2 = 150$

S20. Given at saturation $V_{CE} = 0\,\text{V}, \quad V_{BE} = 0.8\,\text{V}$

$$V_{CE} = V_{CC} - I_C R_C$$
$$I_C = V_{CC}/R_C = 5.0\text{V}/1.0\,\text{k}\Omega = 5.0\,\text{mA}$$

Therefore, $I_B = I_C/\beta = 5.0\,\text{mA}/250 = 20\,\mu\text{A}$

The input voltage at which the transistor will go into saturation is given by

$$V_{IH} = V_{BB} = I_B R_B + V_{BE}$$
$$= 20\,\mu\text{A} \times 100\,\text{k}\Omega + 0.8\,\text{V} = 2.8\,\text{V}$$

The value of input voltage below which the transistor remains cutoff is given by

$$V_{IL} = 0.6\,\text{V}, \quad V_{IH} = 2.8\,\text{V}$$

Between 0.0 V and 0.6 V, the transistor will be in the 'switched off' state. Between 2.8 V and 5.0 V, it will be in 'switched on' state.

Note that the transistor is in active state when I_B varies from 0.0 mA to 20 mA. In this range, $I_C = \beta I_B$ is valid. In the saturation range, $I_C \leq \beta I_B$.

S21. The output a.c. voltage is 2.0 V. So, the a.c. collector current i_C = 2.0/2000 = 1.0 mA. The signal current through the base is, therefore given by $i_B = i_C/\beta$ = 1.0 mA/100 = 0.010 mA. The d.c. base current has to be 10×0.010 = 0.10 mA.

From Eq.14.16, $R_B = (V_{BB} - V_{BE})/I_B$.

Assuming V_{BE} = 0.6 V,

$R_B = (2.0 - 0.6)/0.10 = 14\ \text{k}\Omega$.

The d.c. collector current $I_C = 100 \times 0.10 = 10$ mA.

S22. Given: $\beta_{a.c.} = 20$; $R_{in} = 2\,\text{k}\Omega$ and $R_{out} = 5\,\text{k}\Omega$

$\therefore$ Resistance gain = $\frac{R_{out}}{R_{in}} = \frac{5}{2}$ = **2.5**

(a) Now, voltage gain = $\beta_{a.c.} \times$ resistance gain

= 20×2.5 = **50**

(b) Also, power gain = $\beta^2_{a.c.} \times$ resistance gain

= $20^2 \times 2.5$ = **1,000**.

S23. α and β are known as current gains of a common base amplifier and common emitter amplifier respectively.

To define α: It is defined as the ratio of change in collector current to the change in emitter current at constant collector voltage.

To define β: It is defined as the ratio of change in collector current to the change in base current at constant emitter current.

S24. When the first half cycle of a.c. input voltage is positive. It will make base more positive. Thus, negative forward bias of emitter will increase. it will increase the emitter current and hence the collector current. The increase in collector current will increase potential drop across load resistance and the collector voltage will decrease. As collector is connected to positive pole of the battery, the decrease in collector voltage means that collector will become less positive *i.e.*, negative output signal will be obtained. Thus, corresponding to the positive half cycle of a.c. input, negative output half cycle will be obtained.

S25. In a transistor, the function of the emitter and collector is same as that of the cathode and anode plate respectively in a triode valve. The emitter will send charge carries (electrons or holes) towards this base only, when it is forward-biased. on the other hand, the collector will collect them, when it is reverse-biased.

S26. To use a transistor as a rectifier, either its emitter-base portion or the collector-base portion has to be used. Since base is thin and lightly doped, either of the two portions will not work as *p-n* junction diode. Hence, a transistor cannot be used as a rectifier.

S27. (a) The collector current will become ***smaller***. It is because, more majority carries going from emitter to collector will recombine in base.

(b) Because of the above reason, base current will become ***larger***.

S28. Given: $R_{in} = 1{,}000\ \Omega$; $R_{out} = 5\ k\Omega = 5 \times 10^3\ \Omega$ and when $\Delta I_b = 10\ \mu A = 10 \times 10^{-6}$ A, $\Delta I_c = 2\ mA = 2 \times 10^{-3}$ A

(a) Now, current gain,

$$\beta_{a.c.} = \frac{\Delta I_c}{\Delta I_b} = \frac{2 \times 10^{-3}}{10 \times 10^{-6}} = \mathbf{200}$$

(b) Also, voltage gain,

$$A_v = \beta_{a.c.} \times \frac{R_{out}}{R_{in}}$$

$$= -200 \times \frac{5 \times 10^3}{1{,}000} = \mathbf{-1{,}000}$$

The negative sign shows that output is out of phase with the input.

S29. Given: $\alpha = 0.96$; $I_e = 7.2$ mA

Now, $\alpha = \frac{I_c}{I_e}$ or $I_c = \alpha I_e = 0.96 \times 7.2 = 6.91$ mA

Also, $I_e = I_c + I_b$ or $I_b = I_e - I_c = 7.2 - 6.91 = 0.29$ mA

S30. From the relation: $I_e = I_c + I_b$

We have

$$\Delta I_e = \Delta I_c + \Delta I_b$$

When

$\Delta I_e = 8.0$ mA, $\Delta I_c = 7.9$ mA

$\therefore$ $\Delta I_b = \Delta I_e - \Delta I_c = 8.0 - 7.9 = \mathbf{0.1\ mA}$

Also, $\alpha = \frac{\Delta I_c}{\Delta I_e} = \frac{7.9}{8.0} = \mathbf{0.9875}$

Further, $\beta = \frac{\Delta I_c}{\Delta I_b} = \frac{7.9}{0.1} = \mathbf{79}$.

S31. The given figure in question is common Emitter (*CE*) configuration of an *n-p-n* transistor. The input circuit is forward biased and collector circuit is forward biased and collector circuit is reverse biased.

As the base resistance *R* decreases, the input circuit will become more forward biased thus decreasing the base current (I_B) and increasing the emitter current (I_E). This will increase the collector current (I_C) as $I_E = I_B + I_C$.

When I_C increases which flows through the lamp, the voltage across the bulb will also increase thus making the lamp brighter and as the voltmeter is connected in parallel with the lamp, the reading in the voltmeter will also increase.

S32. Lamp glows brighter and voltmeter reading increases with the decrease of *R*. input current increase which in turn by transistor action lead to increase collector current. This makes lamp brighter and hence, voltmeter reading goes up.

S33. In the circuit shown in the above figure (a), the lamp will light. It is because, the *n-p-n* transistor in the circuit can conduct only when its base is positive.

S34. Given: $\Delta I_b = 15\,\mu A = 15 \times 10^{-6}\,A$; $\Delta I_c = 2\,mA = 2 \times 10^{-3}\,A$; $R_{in} = 665\,\Omega$; $R_L = 5\,k\Omega = 5 \times 10^3\,\Omega$

(a) Now, $$\beta_{a.c.} = \frac{\Delta I_c}{\Delta I_b} = \frac{2 \times 10^{-3}}{15 \times 10^{-6}} = \mathbf{133.3}$$

(b) Transconductance, $$g_m = \frac{\beta_{a.c.}}{R_{in}} = \frac{133.3}{665} = \mathbf{0.2\,\Omega^{-1}}$$

(c) Voltage gain, $$A_v = -g_m R_L = -0.2 \times 5 \times 10^3 = \mathbf{-1{,}000}$$

The negative sign shows that output is out of phase with the input.

S35. Given: $\Delta I_b = 20\,\mu A = 20 \times 10^{-6}\,A$; $\Delta V_{be} = 0.02\,V$ and $\Delta I_c = 2\,mA = 2 \times 10^{-3}\,A$

(a) Input resistance $$= \frac{\Delta V_{be}}{\Delta I_b} = \frac{0.02}{20 \times 10^{-6}} = \mathbf{1{,}000\,\Omega}$$

$$\beta = \frac{\Delta I_c}{\Delta I_b} = \frac{2 \times 10^{-3}}{20 \times 10^{-6}} = \mathbf{100}$$

$$g_m = \frac{\Delta I_c}{\Delta V_{be}} = \frac{2 \times 10^{-3}}{0.02} = \mathbf{0.1\,\Omega^{-1}}$$

(b) $R_L = 5\,k\Omega = 5{,}000\,\Omega$

Now, voltage gain, $A_v = -\frac{\Delta V_{ce}}{\Delta V_{be}} = -\frac{R_L \times \Delta I_c}{\Delta V_{be}} = \frac{5{,}000 \times 2 \times 10^{-3}}{0.02} = \mathbf{-500}$

The negative sign shows that output is out of phase with the input.

S36. Collector resistance, R_C = 2 kΩ = 2000 Ω

Audio signal voltage across the collector resistance, V = 2 V

Current amplification factor of the transistor, β = 100

Base resistance, R_B = 1 kΩ = 1000 Ω

Input signal voltage = V_i

Base current = I_B

We have the amplification relation as:

$$\text{Voltage amplification} = \frac{V}{V_i} = \beta \frac{R_C}{R_B}$$

$$V_i = \frac{V}{\beta} \frac{R_C}{R_B} = \frac{2 \times 100}{100 \times 200} = 0.01\,\text{V}$$

Therefore, the input signal voltage of the amplifier is 0.01 V.

Base resistance is given by the relation:

$$R_B = \frac{V_i}{I_B} = \frac{0.01}{1000} = 10 \times 10^{-5}\,\mu\text{A}$$

Therefore, the base current of the amplifier is 10 μA.

S37. (a) Dynamic output resistance is given as

$$R_0 = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_b = \text{constant}} = \frac{12 - 8}{(3.6 - 3.4) \times 10^{-3}}$$

$$= \frac{4}{0.2 \times 10^{-3}} = 20\ k\Omega$$

(b) DC current gain

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{3.5\,\text{mA}}{30\,\mu\text{A}} = \frac{3.5 \times 10^{-3}}{30 \times 10^{-6}}$$

$$= \frac{350}{3} = 116.67$$

(c) AC current gain

$$\beta_{dc} = \frac{\Delta I_C}{\Delta I_B} = \frac{(4.7 - 3.5)\,\text{mA}}{(40 - 30)\,\mu\text{A}}$$

$$= \frac{1.2 \times 10^{-3}}{10 \times 10^{-6}} = 120$$

S38. In the circuit shown in the above figure, then *n-p-n* transistor is forward biased. If resistor *R* is reduced, emitter current I_e will increase. The collector current flowing through the lamp is given by

$$I_c = I_e - I_b.$$

It follows that due to increase in I_e, I_c will also increase. It will lead to make the lamp glow ***more brilliantly***.

The voltmeter *V* measures potential difference across *L*. Due to increase in current through the lamp, potential difference across the lamp and hence reading of the voltmeter will ***increase***.

S39. The collector current will become smaller.

Due to the fact that base is doped lightly, the number density of majority carriers (electrons in *p-n-p* and holes in *n-p-n* transistor) is low. When emitter is forward biased, electron-hole combination takes place in the base region. Since it is thin and lightly doped, only a small amount (about 5%) of electron-hole recombination will take place.

S40. The logic gate marked *X* is ***NAND gate***, while the gate marked as *Y* is ***OR gate***.

From the above figure, it follows that for the inputs *A* and *B*, the output of the *NAND gate* is *y'*. Now, for the *OR gate*, the inputs are *A* and *y'* and the output is *y*. We know that output of *NAND gate* is 0, only when both the inputs are 1 and put of *OR gate* is 1, when either of the two inputs is 1. Keeping these facts in view, the input-output combinations for the given circuit will be as given in table below.

A	*B*	*y'*	*y*
0	1	1	1
1	0	1	1

II[nd] Method: Now, $y' = \overline{A.B}$

$\therefore$ $y = A + \overline{A.B}$

Applying De Morgan's second theorem, we gate

$$y = A + \overline{A} + \overline{B} = 1 + \overline{B} = 1$$

It follows that *y* will be 1, for both the input combinations and hence, above table (read columns *A*, *B* and *y* only) is the truth table for the given logic circuit.

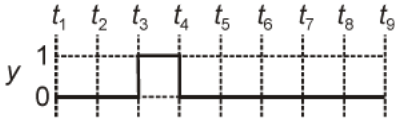
S41. (a) From the figure below, it follows that during different time intervals, the input waveforms *A* and *B* are high (1) and low (0) as tabled below:

Interval	$t_1 - t_2$	$t_2 - t_3$	$t_3 - t_4$	$t_4 - t_5$	$t_5 - t_6$	$t_6 - t_7$	$t_7 - t_8$	$t_8 - t_9$
Input A	0	1	1	0	0	1	1	0
Input B	0	0	1	1	0	0	0	1

The output of AND gate is 1, when both the inputs A and B are 1. Therefore, for the inputs A and B listed above, the output of the AND gate at the various instants will be as below:

Interval	$t_1 - t_2$	$t_2 - t_3$	$t_3 - t_4$	$t_4 - t_5$	$t_5 - t_6$	$t_6 - t_7$	$t_7 - t_8$	$t_8 - t_9$
Output y	0	0	1	0	0	0	0	0

Hence, for the given input waveforms, the output waveform of the AND gate will be as shown in the figure.



(b) Let y' be output of AND gate and y be the output, when the output of AND gate is fed to the NOT gate.

Then, $\quad y' = A \,.\, B \quad$ and $\quad y = \overline{y'}$

$\therefore \quad y = \overline{A.B}$

It is the Boolean expression for a NAND gate.

Hence, when the output of AND gate is fed to a NOT gate, the combination acts as NAND gate.

S42. A NOT gate inverts the input. Because of this, the column y_1 contains 1, when A is 0; and 0, when A is 1. For the same reason, the column y_2 contains 1, when B is 0; and 0, when B is 1. Now, the outputs y_1 and y_2 of the two NOT gates from when either or both the inputs are 1. Therefore, the column y contains 1, when either or both the inputs y_1 and y_2 are 1. Keeping these facts in view, the input-output combinations for the given circuit will be as given in Table (a). Hence, the truth table (read columns A, B and y only in Table (a)) of the given logic circuit will be as Table (b)

Table (a)

A	B	y_1	y_2	y
0	0	1	1	1
1	0	0	1	1
0	1	1	0	1
1	1	0	0	0

$\equiv$

Table (b)

A	B	y
0	0	1
1	0	1
0	1	1
1	1	0

It follows that it is the truth table for a NAND gate (see the table below)

A	B	y
0	0	1
1	0	1
0	1	1
1	1	0

Hence, the combination of gates shown in the above figure behaves as ***NAND gate***.

II[nd] Method: Now, $y_1 = \overline{A}$ and $y_2 = \overline{B}$

$\therefore$ $y = y_1 + y_2$

or $y = \overline{A} + \overline{B}$

Applying De Morgan's first theorem, we get

$y = \overline{A.B}$ $(\because \overline{A.B} = \overline{A} + \overline{B})$

It is the Boolean expression for a NAND gate.

It follows that

when $A = 0;\ B = 0,$ then $y = \overline{0.0} = \overline{0} = 1,$

when $A = 1;\ B = 0,$ then $y = \overline{1.0} = \overline{0} = 1,$

when $A = 0;\ B = 1,$ then $y = \overline{0.1} = \overline{0} = 1,$

when $A = 1;\ B = 1,$ then $y = \overline{1.1} = \overline{1} = 0,$

Therefore, the input-output combinations for the given circuit are as given in Table (a), which is the truth table of a NAND gate.

Hence, the logic circuit functions as ***NAND gate***.

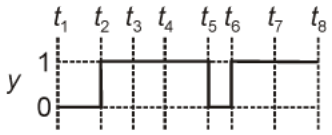
S43. From the above figure, it follows that during different time intervals, the input waveforms A and B are high (1) and low (0) as tabled below:

Interval	$t_1 - t_2$	$t_2 - t_3$	$t_3 - t_4$	$t_4 - t_5$	$t_5 - t_6$	$t_6 - t_7$	$t_7 - t_8$
Input A	0	1	1	0	0	1	0
Input B	0	0	1	1	0	0	1

(a) The output of or gate is 1, when either or both the inputs are 1. Therefore, for the inputs A and B listed above, the output of the OR gate at the various instants will be below.

Interval	$t_1 - t_2$	$t_2 - t_3$	$t_3 - t_4$	$t_4 - t_5$	$t_5 - t_6$	$t_6 - t_7$	$t_7 - t_8$
Output y	0	1	1	1	0	1	1

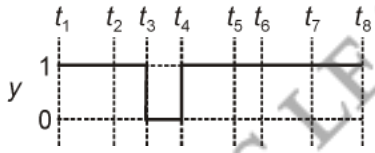
Hence, for the given input waveforms, the output waveform of the OR gate will be as shown in the figure below.



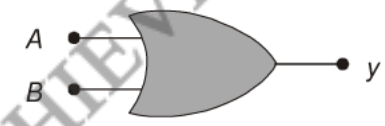
(b) We know that output of NAND gate is 0, only when both the inputs are 1. Therefore, for the inputs A and B listed above, the output of the NAND gate at the various instants will be as below:

Interval	$t_1 - t_2$	$t_2 - t_3$	$t_3 - t_4$	$t_4 - t_5$	$t_5 - t_6$	$t_6 - t_7$	$t_7 - t_8$
Output y	1	1	0	1	1	1	1

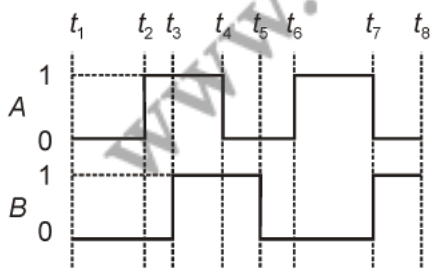
Hence, for the given input waveforms, the output waveform for the NAND gate will be as shown in the figure below.



S44. **Logic Symbol:** As shown in the figure below



The input signal has been analysed in the figure below:



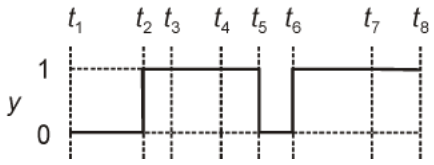
From the above figure, it follows that during different time intervals, the input waveforms A and B are high (1) and low (0) as tabled below:

Interval	$t_1 - t_2$	$t_2 - t_3$	$t_3 - t_4$	$t_4 - t_5$	$t_5 - t_6$	$t_6 - t_7$	$t_7 - t_8$
Input *A*	0	1	1	0	0	1	0
Input *B*	0	0	1	1	0	0	1

For an OR gate, the output is high (1), when either or both the inputs are high (1). Therefore, for the inputs *A* and *B* listed above, the output of the OR gate at the various instants will be as below:

Interval	$t_1 - t_2$	$t_2 - t_3$	$t_3 - t_4$	$t_4 - t_5$	$t_5 - t_6$	$t_6 - t_7$	$t_7 - t_8$
Output *y*	0	1	1	1	0	1	1

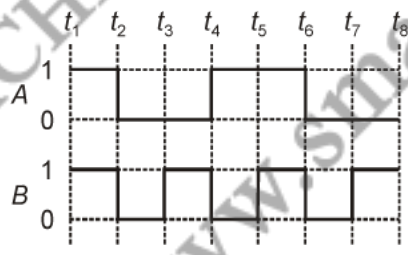
Hence, the output waveform of the OR gate for the given input waveform will be as shown in the figure below



S45. The circuit symbol shown in above figure (a) represents the ***AND gate***. Its truth table is as given by table below.

A	*B*	*y*
0	0	0
1	0	0
0	1	0
1	1	1

The input signal has been analysed in the figure (c).



(c)

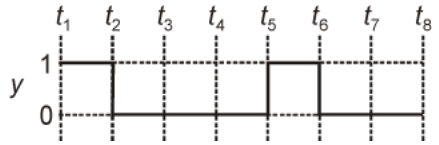
From the figure (c), it follows that during different time intervals, the input waveforms *A* and *B* are high (1) and low (0) as tabled below:

Interval	$t_1 - t_2$	$t_2 - t_3$	$t_3 - t_4$	$t_4 - t_5$	$t_5 - t_6$	$t_6 - t_7$	$t_7 - t_8$
Input *A*	1	0	0	1	1	0	0
Input *B*	1	0	1	0	1	0	1

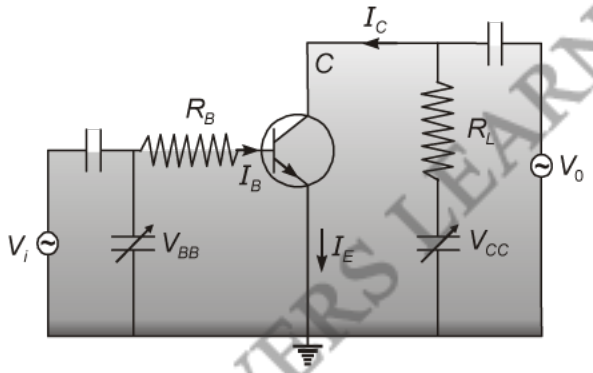
For an AND gate, the output is high (1), when both the inputs are high (1). Therefore, for the inputs *A* and *B* listed above, the output of the AND gate at the various instants will be as below:

Interval	$t_1 - t_2$	$t_2 - t_3$	$t_3 - t_4$	$t_4 - t_5$	$t_5 - t_6$	$t_6 - t_7$	$t_7 - t_8$
Output *y*	1	0	0	0	1	0	0

Hence, the output waveform of the AND gate for the given input waveform will be as shown in the figure (d).



S46.



When transistor acts as an amplifier it operates in active region.

When an a.c. input signal V_i is superimposed on the bias V_{BB}, the output, which is measured between collector and ground, increases.

$$V_{CC} = V_{CE} + I_C R_L$$
$$V_{BB} = V_{BE} + I_B R_B$$

When U_i is non zero, we get

$$V_{BB} + V_i = V_{BE} + I_B R_B + \Delta I_B (R_B + R_i)$$

$$V_i = \Delta I_B (R_B + R_i)$$
$$V_i = r \Delta I_B \quad \text{... (i)}$$

Change in I_B cause a change in I_C

So $$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}$$

As $$\Delta V_{CC} = \Delta V_{CE} + R_L \Delta I_C$$

$$\Delta V_{CE} = -R_L \Delta I_C \qquad [\because \ \Delta V_{CC} = 0]$$

$$V_0 = -R_L \Delta I_C \qquad [\because \ \Delta V_{CE} = V_0]$$

$$V_0 = -R_L (\beta_{ac} \Delta I_B) \qquad [\because \ \Delta I_C = \beta_{ac} \Delta I_B] \quad \text{... (ii)}$$

From Eqn. (i) and (ii), we get

Voltage gain of the amplifier

$$A_V = \frac{V_0}{V_i} = \frac{\Delta V_{CE}}{r \Delta I_B}$$

$$A_V = \frac{-\beta_{ac} \Delta I_B R_L}{r \Delta I_B}$$

$$A_V = -\beta_{ac} \frac{R_L}{r}$$

Negative sign in the above expression indicates that output signal is having a phase difference of 'π' w.r.t input signal.

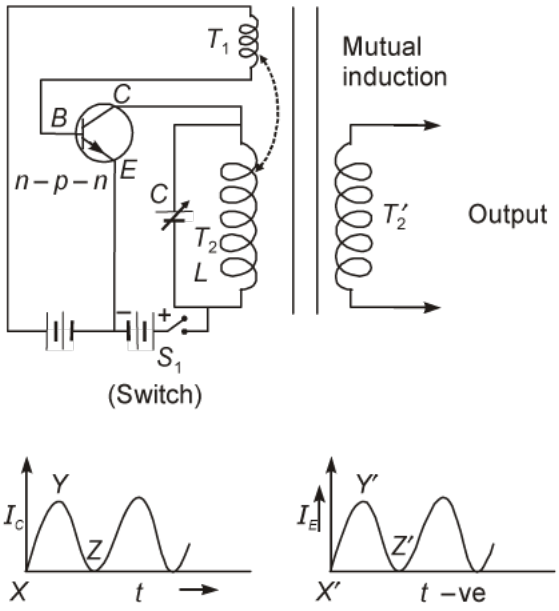
S47.(a) **Principle:** A portion of the output power from an amplifier if returned to input in phase sustained a.c signals are obtained.

Oscillator circuit is made 'up' of three parts.

(i) Tank circuit (*LC* circuit) (ii) Amplifier circuit (iii) Feedback circuit (inductive coupling)

As soon as switch *s*, is on, collector current start increasing from *X* to *Y*, inductive coupling between coil T_2 and T_1 causes a current to flow in the emitter circuit. This current (I_E) increases from *X'* to *Y'*. When current in T_2 acquires the value *Y* transistor becomes saturated. As 'I_C' does not change, magnetic field around T_C causes to grow *i.e.*, no further feedback from T_2 to T_1. Without continuous feedback, emitter current begins to fall from *Y* to *Z*. With this magnetic field around T_2 decays. This further decreases emitter current till it reaches *Z* when the transistor is in cut-off state the whole process now repeats itself again and again. The time for change from saturation to cut-off and back is determined by the constants of the tank circuit. The frequency of this tuned circuit is

$$f = \frac{1}{2\pi\sqrt{LC}}$$



(b) AND gate

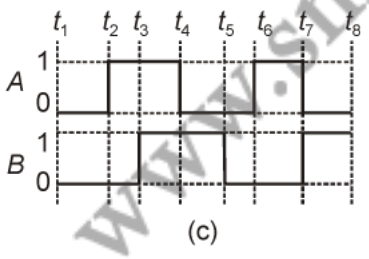
$$\overline{\overline{A} + \overline{B}} = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

S48. The circuit symbol shown in the figure (a) represents the ***NOR gate*** and its truth table is as given by table below

A	B	y
0	0	1
1	0	0
0	1	0
1	1	0

The input signal has been analysed in the figure (c).



(c)

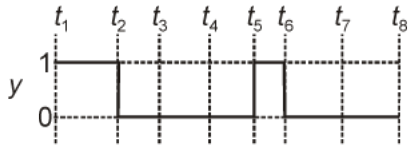
From the figure (d), it follows that during different time intervals, the input waveforms *A* and *B* are high (1) and low (0) as tabled below:

Interval	$t_1 - t_2$	$t_2 - t_3$	$t_3 - t_4$	$t_4 - t_5$	$t_5 - t_6$	$t_6 - t_7$	$t_7 - t_8$
Input A	0	1	1	0	0	1	0
Input B	0	0	1	1	0	0	1

For a NOR gate, the output is high (1), only when both the inputs are low (0). Therefore, for the inputs A and B listed above, the output of the NOR gate at the various instants will be as below:

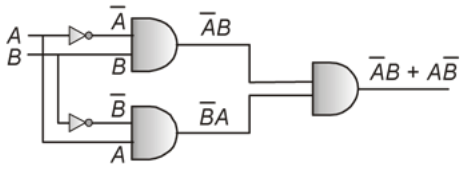
Interval	$t_1 - t_2$	$t_2 - t_3$	$t_3 - t_4$	$t_4 - t_5$	$t_5 - t_6$	$t_6 - t_7$	$t_7 - t_8$
Output y	1	0	0	0	1	0	0

Hence, the output waveform of the NOR gate for the given input waveform will be as shown in the figure below.

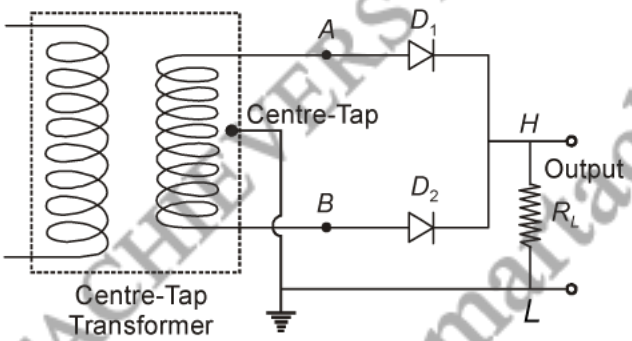


(d)

S49.

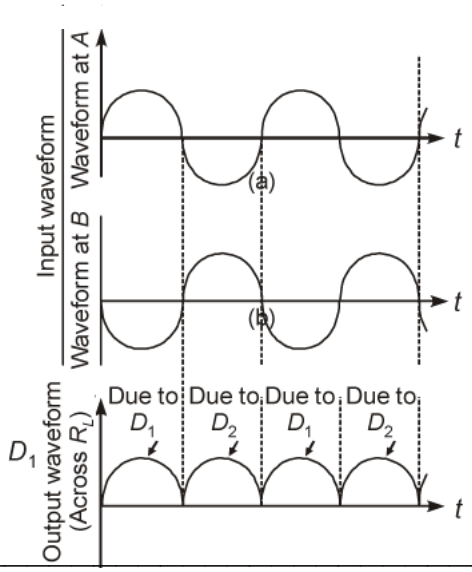


S50. (a)

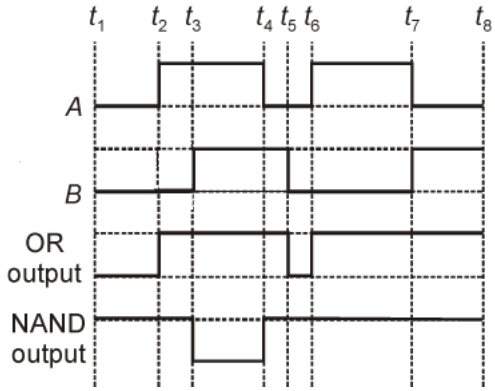


During first half of the cycle if A is at +ve potential w.r.t. centre tap and B is at –ve potential. Diode D_1 being forward biased conducts and diode D_2 being reverse biased does not conduct. Current flows through the load in the sense H to L. During second half of the cycle conditions get reversed. Only diode D_2 conducts. Again current flows through load in the sense H to L.

Thus, in the output we get unidirectional current.



(b)



S51. As $V_{be} = 0$, potential drop across R_b is 10 V.

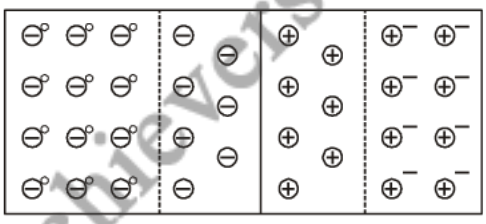
$$\therefore \quad I_b = \frac{10}{400 \times 10^3} = 25\,\mu A$$

Since $V_{ce} = 0$, potential drop across R_c, *i.e.*, $I_c R_c$ is 10 V.

$$\therefore \quad I_c = \frac{10}{3 \times 10^3} = 3.33 \times 10^{-3} = 3.33 \text{ mA}.$$

$$\therefore \quad \beta = \frac{I_c}{I_b} \frac{3.33 \times 10^{-3}}{25 \times 10^{-6}} = 1.33 \times 10^2 = 133.$$

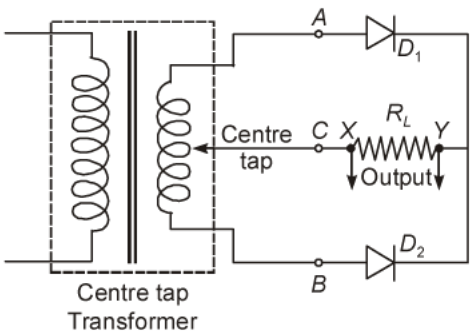
S52. (a) As soon as a *p-n* junction is formed diffusion of charges take place from higher concentration to lower concentration. On crossing the *p-n* boundary, these electrons and holes may collide with each other and recombine (or annihilate). As these electrons/holes come from donor or acceptor impurity atom cores, such donor or acceptor atoms get depleted of their free charges. Only charged ion core is left in the layer near the junction boundary. This layer is called depletion layer.



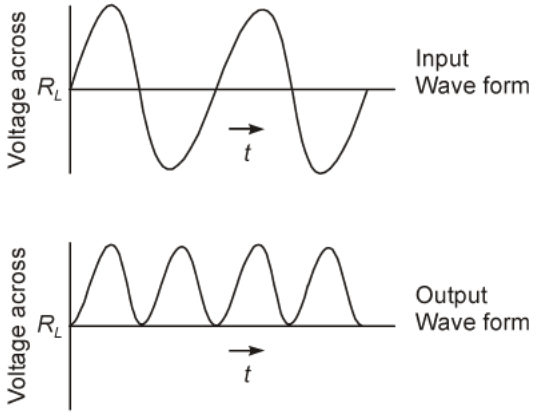
On the *n*-side near the junction, there is a layer of charged donor atom cores with effective +ve charge. On the *p*-side there are charged acceptor atom cores with effective –ve charge. This charge accumulation creates a junction potential. This junction, potential opposes any further diffusion of the majority charge barriers. So, this is called barrier potential.

(b) *p-n* junction diode as a full wave rectifier

We use centre-tap transformer in which the voltages at any instant at *A* and *B* w.r.t. the centre tap are out of phase with each other. Suppose input voltage to *A* at any instant is +ve. Voltage at *B* will be –ve. Diode D_1 will get forward biased and D_2 will get reverse biased. During this cycle we get output current



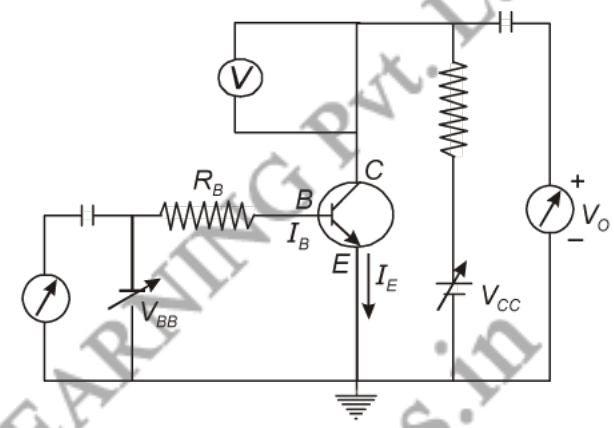
flowing Y to X. Thus output voltage across R_L. When voltage at A becomes negative then the voltage at B would be +ve. Diode D_2 will conduct and D_1 will not conduct. Current will flow Y to X through load resistance. Do, we get output voltage during the +ve as well as –ve half of the cycle.



(c) It is AND gate

A	B	$\overline{A.B} = Y_1$	$Y_2 = \overline{Y}_1$
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

S53. (a) Circuit is shown in the figure:



Current amplification factor (β_{AC}) is the ratio of change in collector current (ΔI_C) to the change is based current (ΔI_B) at constant collector voltage *i.e.*,

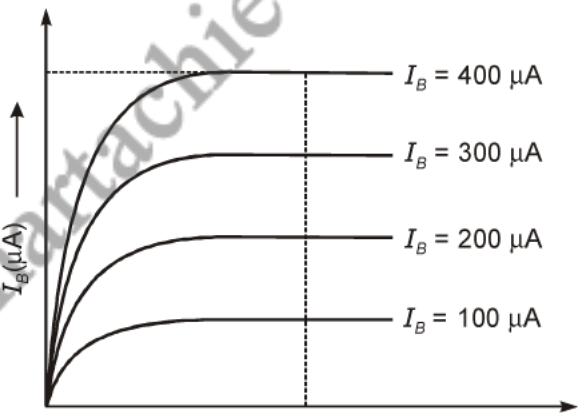
$$\therefore \quad \beta_{AC} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{AC}\text{ = constant}}$$

Output characteristics represent the variation of I_C, with I_B keeping I_B constant.

From the graph at $V_C = V$, the value of collector current increase with the increase in the base current, I_B.

Thus, $$\beta_{AC} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{AC}\text{ = constant}}$$

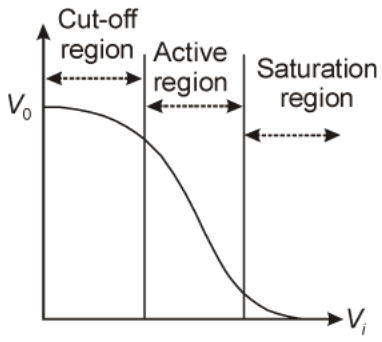
[AC current gain]



(b) Transfer characteristics curve, for a base-biased transistor in *CE* configuration.

In cut-off region and in saturation region transistor acts as switch off and switch on respectively.

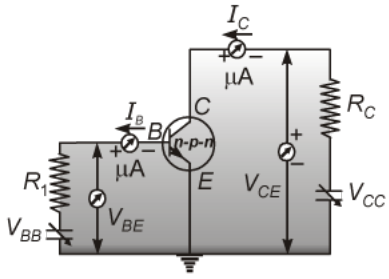
In this region, as long as V_i is low, it enables to forward bias the transistor and enables to forward bias the transistor and V_0 is high. Transistor is not conducting in this region. Hence, it is said to be switched off.



In saturation region, V_i is high enough to live the transistor, the V_0 is low. It is said to be stretched on.

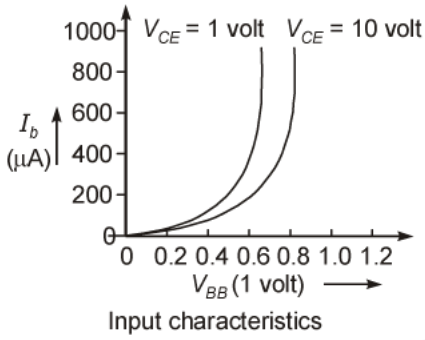
Hence, low input give high output and high input gives low output.

S54. (a)



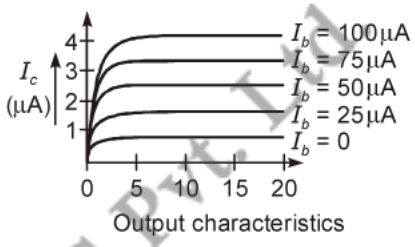
Common emitter configuration of *n-p-n* transistor

(a)



Input characteristics

(b)



Output characteristics

(c)

(b) In the common emitter or grounded emitter configuration, the input signal is applied across the base and the emitter, while the amplified output signal is taken across the collector and the emitter.

This is the most efficient amplifier circuit. Its input resistance is some what higher and the output resistance is lower than those of the common base circuit. It provides the highest voltage and power gains. Apply Kirchhoff's law to input loop, (Assume input voltage V_i is zero) then

$$V_{BB} = V_{BE} + I_B R_B \quad \text{... (i)}$$

Similarly for output loop,

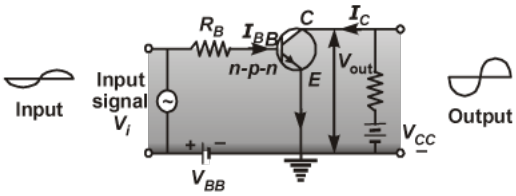
$$V_{CC} = V_{CE} + I_C R_L \quad \text{... (ii)}$$

When input voltage is not zero, we get

$$V_{BE} + V_i = V_{BE} + I_B R_B$$

and $$V_i = \Delta I_B (R_B + R_i) = R \Delta I_B$$

The change in base current I_B causes a change in collector current I_C.



The d.c. current gain is defined as the ratio of the collector-current to the base current and is denoted by β (d.c).

$\therefore$ β (d.c) = I_C / I_B.

The (a.c.) current gain is defined as the ratio of the change in the collector-current to the change in the base-current at a constant collector-to-emitter voltage.

$\therefore$ β (d.c) = $(\Delta I_C / \Delta I_B)_{V_{CE}}$.

The change in I_C due to change in I_B causes a change in V_{CE} and the voltage drop across the output load resistor R_L. Since the amplifier work in the middle of the linear part of its active region, V_{CC} is fixed.

$\therefore$ From Eq. (ii), we get

$$\Delta V_{CC} = 0 \rightarrow \Delta V_{CE} = -R_L \Delta I_C$$

The voltage gain of the amplifier is

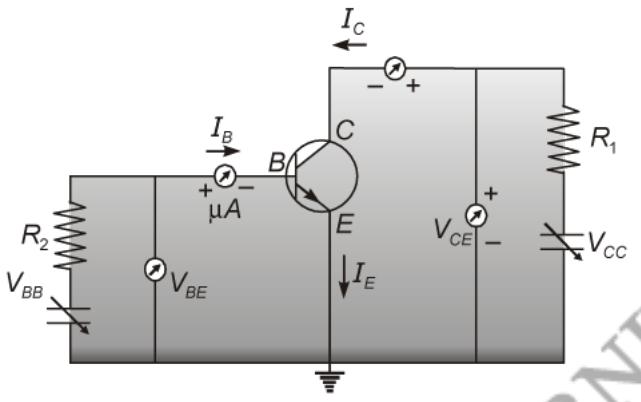
$$A_V = \frac{\text{Output voltage}}{\text{Input voltage}} = \frac{V_0}{V_i} = \frac{\Delta V_{CE}}{R \Delta I_B} = -\frac{\beta_{ac} . R_L}{R}.$$

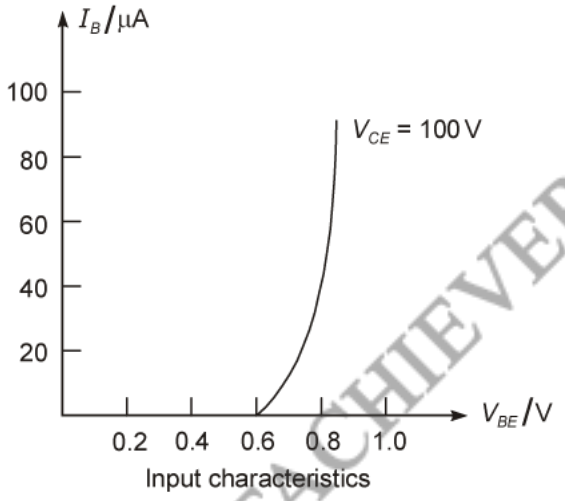
Negative sign shows that output voltage is opposite with the input voltage.

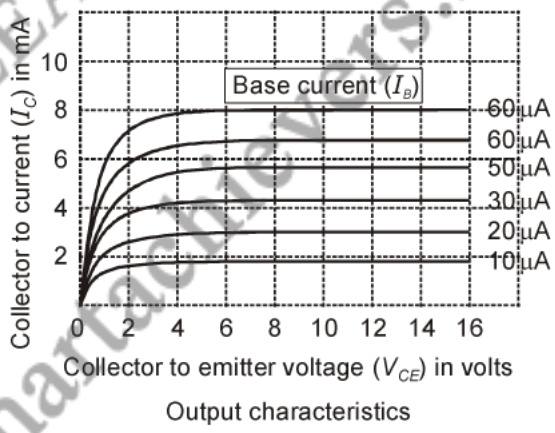
Thus the phase change between the input and output is 180°.

This is caused due to variation in collector current caused by biasing change in input side.

S55. (a)





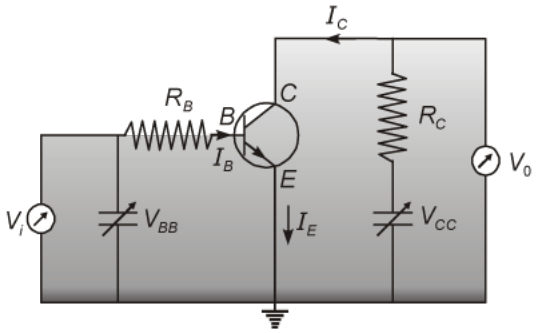


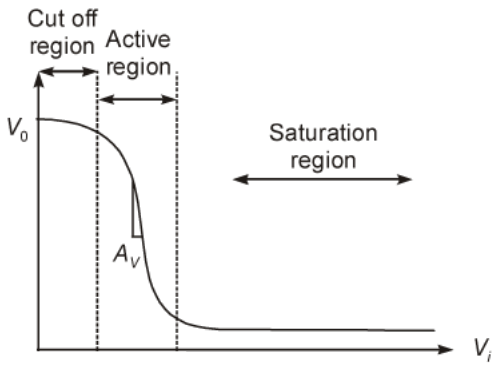
For determination of β_{ac} consider any two characteristics for two values of I_B on either side of the given value of I_C. To find out ΔI_B. Now, find out corresponding values of I_C at a given value of V_{CE}. To calculate ΔI_C. Use the relation

$$\beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$$

To find out β_{ac}.

(b)





For using transistor as a switch we operate it in cut off and saturation region.

S56. From the output characteristics at point Q,

$$V_{CE} = 8\,\text{V} \quad \text{and} \quad I_C = 4\,\text{mA}$$

$$V_{CC} = I_C R_C + V_{CE}$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C}$$

$$R_C = \frac{16 - 8}{4 \times 10^{-3}} = 2\,\text{K}\Omega$$

Since, $V_{BB} = I_B R_B + V_{BE}$

$$R_B = \frac{16 - 0.7}{30 \times 10^{-6}} = 510\,\text{K}\Omega$$

Now, $$\beta = \frac{I_C}{I_B} = \frac{4 \times 10^{-3}}{30 \times 10^{-6}} = 133$$

Voltage gain $$A_V = -\beta \frac{R_C}{R_B} = -133 \times \frac{2 \times 10^3}{510 \times 10^3} = -0.52$$

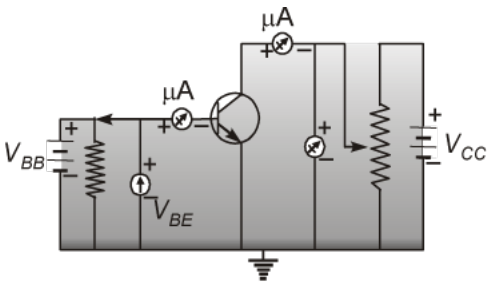
Power gain $$A_P = \beta \times A_V = -\beta^2 \frac{R_C}{R_B} = (133)^2 \times \frac{2 \times 10^3}{510 \times 10^3} = \mathbf{69}.$$

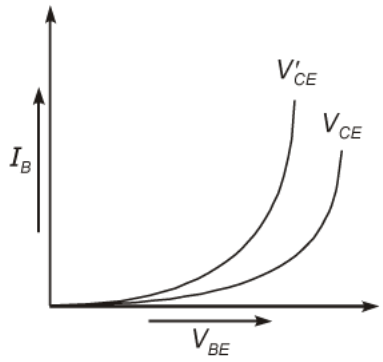
S57. Base region controls the flow of majority charge carriers through a transistor.

Base region is made thin and lightly doped so that the probability of majority charge carriers being captured is minimum. Base current get reduced and collector current is increased.

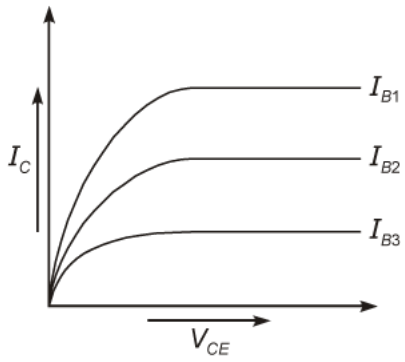
When I_C increases amplification action of the transistor also increases.

Circuit to study transistor characteristics.





Input characteristics



Output characteristics

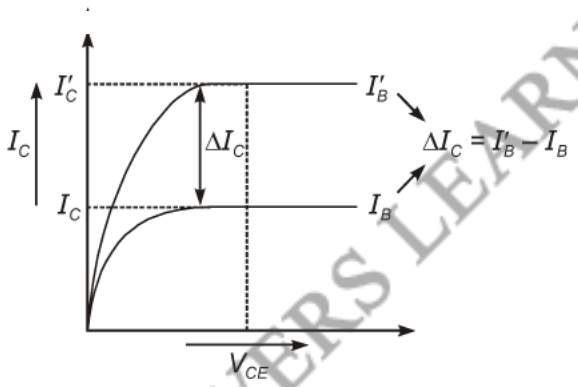
Current amplification factor (β) is the ratio of change in collector current (output current) to the change in base current.

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CB}}.$$

To calculate 'β' from output characteristics

(a) Consider characteristics for any two values of I_B.

(b) For a given value of V_{CE} find out two values of I_C on the above two characteristics.

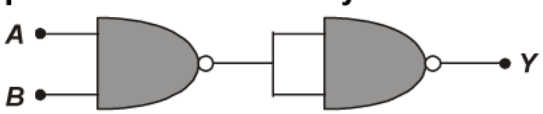


(c) Substitute values and calculate *B*.

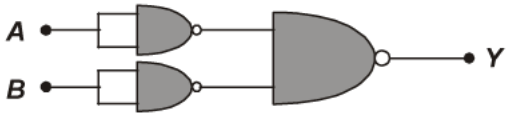
$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}.$$

Date: 22/10/2021

Q1. You are given two circuits as shown in figure, which consist of NAND gates. Identify the logic operation carried out by the two circuits.

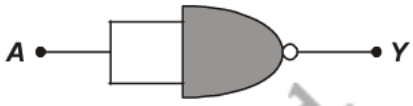


(a)



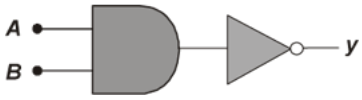
(b)

Q2. Write the truth table for a NAND gate connected as given in figure.



Hence identify the exact logic operation carried out by this circuit.

Q3. Write the truth table for the combination of gates shown here.

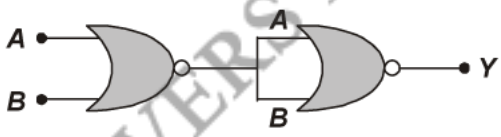


Q4. What is the difference between analog and digital circuits?

Q5. State the relation between the frequency ν of radiation emitted by LED and the band gap energy *E*, of the semiconductor used to fabricate it.

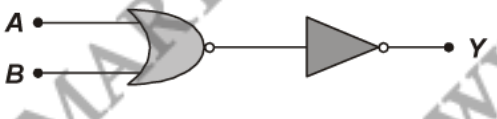
Q6. State the reason, why GaAs is most commonly used in making of a solar cell.

Q7. Write the truth table for circuit given in figure below consisting of NOR gates and identify the logic operation (OR, AND, NOT) which this circuit is performing.

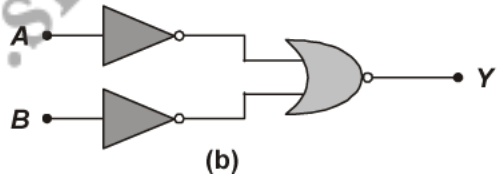


(Hint: *A* = 0, *B* = 1 then *A* and *B* inputs of second NOR gate will be 0 and hence *Y* = 1. Similarly work out the values of *Y* for other combinations of *A* and *B*. Compare with the truth table of OR, AND, NOT gates and find the correct one.)

Q8. You are given the two circuits as shown in figure. Show that circuit (a) acts as OR gate while the circuit (b) acts as AND gate.



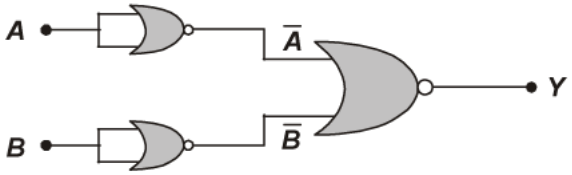
(a)



(b)

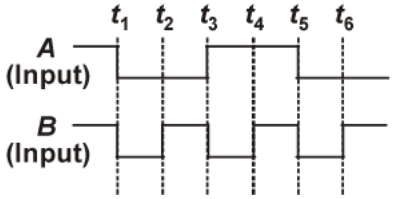
Q9. Write the truth table for the circuits given in figure consisting of NOR gates only. Identify the logic operations (OR, AND, NOT) performed by the two circuits.

(a)

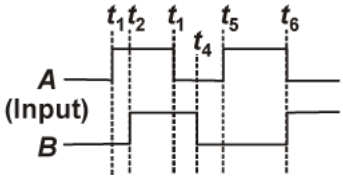


(b)

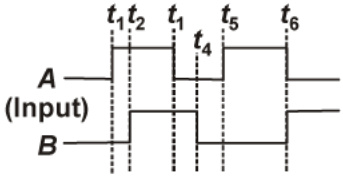
Q10. Sketch the output *Y* from a NAND gate having inputs *A* and *B* given below:



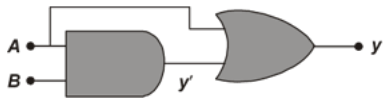
Q11. Justify the output waveform (*Y*) of the OR gate for the following inputs *A* and *B* given in figure.



Q12. Take *A* and *B* input waveforms similar to that in Example 14.11. Sketch the output waveform obtained from AND gate.

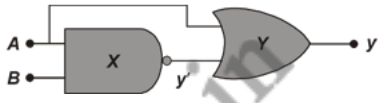


Q13. Write the truth table for the following combination of gates shown in the figure.



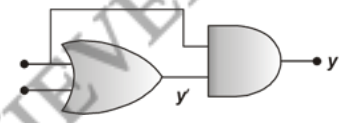
Q14. (a) Describe the working of Light Emitting Diodes (LEDs).
(b) Which semiconductors are preferred to make LEDs and why?
(c) Give two advantages of using LEDs over conventional incandescent low power lamps.

Q15. Identify the logic gates marked X, Y in the figure.
Write down the output at *y*, when *A* = 0, *B* = 0 and *A* = 1, *B* = 1.

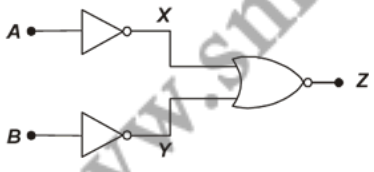


Q16. Draw a circuit diagram showing the biasing of an LED. State the factor which controls
(a) wavelength of light.
(b) intensity of light emitted by the diode.

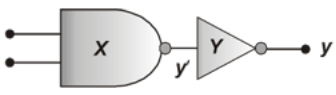
Q17. Write the truth table for the combination of gates shown in the figure.



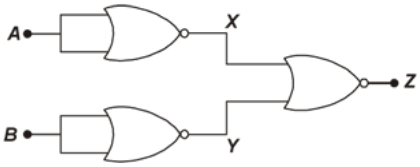
Q18. You are given a circuit below. Write its truth table. Hence, identify the logic operation carried out by this circuit. Draw the logic symbol of the gate it corresponds to.



Q19. Identify the logic gates marked *X*, *Y* in the figure below.
Write down the output at y, when *A* = 1, *B* = 1 and *A* = 0, *B* = 0.



Q20. You are given a circuit below. Write its truth table. Hence, identify the logic operation carried out by this circuit. Draw the logic symbol of the gate it corresponds to.



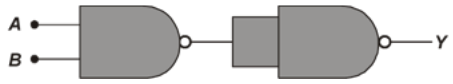
Q21. Draw transfer characteristics of a common emitter *n-p-n* transistor. Point out the region in which the transistor operates as an amplifier. Define the following terms used in transistor amplifiers:

(a) Input resistance (b) Output resistance (c) Current amplification factor.

Q22. Explain briefly with the help of a circuit diagram, the working principle of a transistor amplifier as an oscillator.

Q23. (a) Using the necessary circuit diagram, draw, the transfer characteristics of a base-biased transistor in CE configuration. With the help of these characteristics, explain briefly how the transistor can be used as an amplifier?

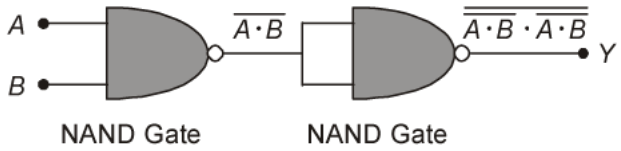
(b) Why are NAND gate called universal gates? Identify the logic operations carried out by the circuit, given below.



Date: 22/10/2021

S1. In both the given circuits, A and B are the inputs and Y is the output.

The output of the left NAND gate will be $\overline{A \cdot B}$, as shown in the following figure.

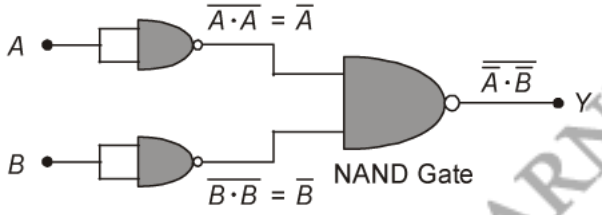


Hence, the output of the combination of the two NAND gates is given as:

$$Y = \overline{(\overline{A \cdot B}) \cdot (\overline{A \cdot B})} = \overline{\overline{AB}} + \overline{\overline{AB}} = AB$$

Hence, this circuit functions as an AND gate.

$\overline{A}$ is the output of the upper left of the NAND gate and $\overline{B}$ is the output of the lower half of the NAND gate, as shown in the following figure.

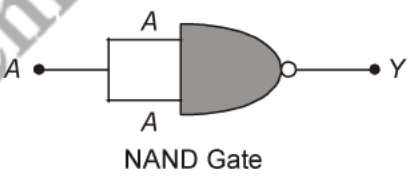


Hence, the output of the combination of the NAND gates will be given as:

$$Y = \overline{A} \cdot \overline{B} = \overline{\overline{A}} + \overline{\overline{B}} = A + B$$

Hence, this circuit functions as an OR gate.

S2. A acts as the two inputs of the NAND gate and Y is the output, as shown in the following figure.



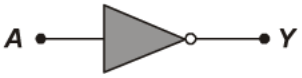
Hence, the output can be written as:

$$Y = \overline{A \cdot A} = \overline{A} + \overline{A} = \overline{A} \quad \ldots \text{(i)}$$

The truth table for equation (i) can be drawn as:

A	$Y (= \overline{A})$
0	1
1	0

This circuit functions as a NOT gate. The symbol for this logic circuit is shown as:



S3.

A	B	Output of AND gate $Y = A.B$	Final output $Y = \overline{Y}'$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

S4. Analog circuits deal with any type of electronic pulses whereas digital circuits deal with square type voltage variation.

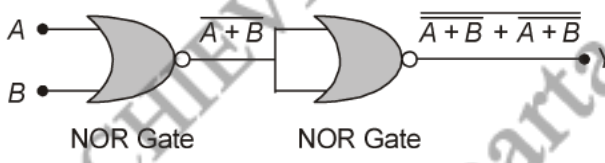
S5. In LED, energy of the photon should be equal to or less than the band gap energy *i.e.*,

$$h\nu \leq E_g$$

where E_g = band gap energy, ν = frequency of emitted photon.

S6. The energy for the maximum intensity to the solar radiation is nearly 1.5 eV. In order to have photo excitation the energy or radiation ($h\nu$) must be greater than energy band gap (E_g). Therefore, the semiconductor with energy band gap about 1.5 eV or lower than it and with higher absorption coefficient is likely to give better solar conversion efficiency. The energy band gap for Si is about 1.1 eV. while for GaAs, it is about 1.53 eV. The GaAs is batter inspite of its higher band gap than Si is about 1.1 eV while for GaAs, it is about 1.53 eV. The GaAs is better inspite of its higher band gap than Si because it absorbs relatively more energy from the incident solar radiations being of relatively higher absorption coefficient.

S7. A and B are the inputs of the given circuit. The output of the first NOR gate is $\overline{A+B}$. It can be observed from the following figure that the inputs of the second NOR gate become the out put of the first one.



Hence, the output of the combination is given as:

$$Y = \overline{\overline{A+B}+\overline{A+B}} = \overline{A}\cdot\overline{B} + \overline{A}\cdot\overline{B}$$

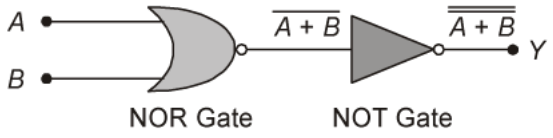
$$= \overline{\overline{A}\cdot\overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} + A + B$$

The truth table for this operation is given as:

A	B	$Y (= A + B)$
0	0	0
0	1	1
1	0	1
1	1	1

This is the truth table of an OR gate. Hence, this circuit functions as an OR gate.

S8. A and B are the inputs and Y is the output of the given circuit. The left half of the given figure acts as the NOR Gate, while the right half acts as the NOT Gate. This is shown in the following figure.



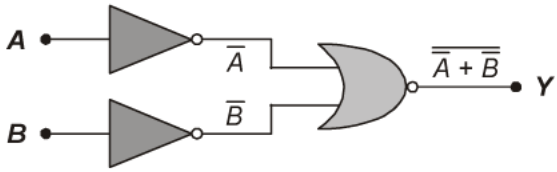
Hence, the output of the NOR Gate = $\overline{A+B}$

This will be the input for the NOT Gate. Its output will be $\overline{\overline{A+B}} = A + B$.

$\therefore$ $Y = A + B$

Hence, this circuit functions as an OR Gate.

A and B are the inputs and Y is the output of the given circuit. It can be observed from the following figure that the inputs of the right half NOR Gate are the outputs of the two NOT Gates.

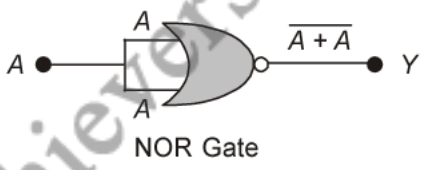


Hence, the output of the given circuit can be written as:

$$Y = \overline{\overline{A}+\overline{B}} = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$$

Hence, this circuit functions as an AND Gate.

S9. A acts as the two inputs of the NOR gate and Y is the output, as shown in the following figure. Hence, the output of the circuit is $\overline{A+A}$.



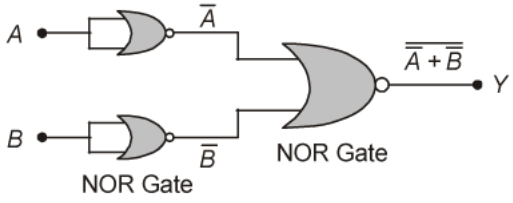
Output, $Y = \overline{A+A} = \overline{A}$

The truth table for the same is given as:

A	$Y (= \overline{A})$
0	1
1	0

This is the truth table of a NOT gate. Hence, this circuit functions as a NOT gate.

A and B are the inputs and Y is the output of the given circuit. By using the result obtained in solution **(a)**, we can infer that the outputs of the first two NOR gates are $\overline{A}$ and $\overline{B}$, as shown in the following figure.



$\overline{A}$ and $\overline{B}$ are the inputs for the last NOR gate. Hence, the output for the circuit can be written as:

$$Y = \overline{\overline{A}+\overline{B}} = \overline{\overline{A}} \cdot \overline{\overline{B}} + A + B$$

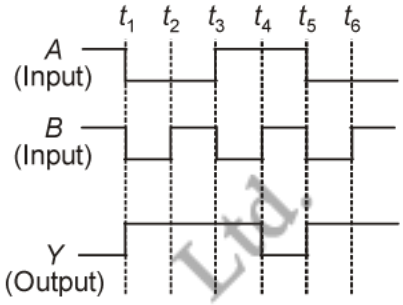
The truth table for the same can be written as:

A	B	$Y (= A \cdot B)$
0	0	0
0	1	1
1	0	1
1	1	1

This is the truth table of an AND gate. Hence, this circuit functions as an AND gate.

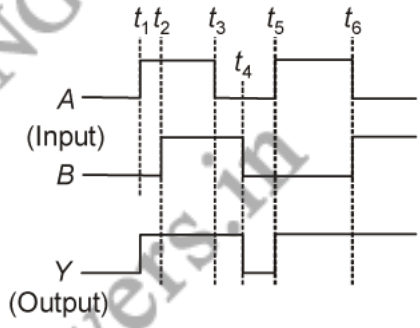
S10. Note the following:

- For $t < t_1$; $A = 1$, $B = 1$; Hence $Y = 0$
- For $t1$ to t_2; $A = 0$, $B = 0$; Hence $Y = 1$
- For $t2$ to t_3; $A = 0$, $B = 1$; Hence $Y = 1$
- For $t3$ to t_4; $A = 1$, $B = 0$; Hence $Y = 1$
- For $t4$ to t_5; $A = 1$, $B = 1$; Hence $Y = 0$
- For $t5$ to t_6; $A = 0$, $B = 0$; Hence $Y = 1$
- For $t > t_6$; $A = 0$, $B = 1$; Hence $Y = 1$



S11. Note the following:

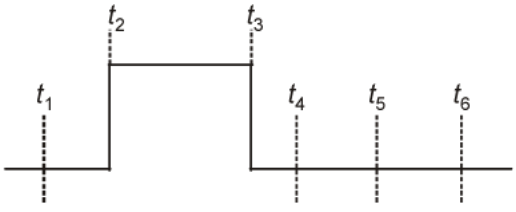
- At $t < t_1$; $A = 0$, $B = 0$; Hence $Y = 0$
- For t_1 to t_2; $A = 1$, $B = 0$; Hence $Y = 1$
- For t_2 to t_3; $A = 1$, $B = 1$; Hence $Y = 1$
- For t_3 to t_4; $A = 0$, $B = 1$; Hence $Y = 1$
- For t_4 to t_5; $A = 0$, $B = 0$; Hence $Y = 0$
- For t_5 to t_6; $A = 1$, $B = 0$; Hence $Y = 1$
- For $t > t6$; $A = 0$, $B = 1$; Hence $Y = 1$



Therefore the waveform Y will be as shown in the figure.

S12. Note the following:

- For $t \leq t_1$; $A = 0$, $B = 0$; Hence $Y = 0$
- For t_1 to $t2$; $A = 1$, $B = 0$; Hence $Y = 0$
- For t_2 to $t3$; $A = 1$, $B = 1$; Hence $Y = 1$
- For t_3 to t_4; $A = 0$, $B = 1$; Hence $Y = 0$
- For t_4 to t_5; $A = 0$, $B = 0$; Hence $Y = 0$
- For t_5 to t_6; $A = 1$, $B = 0$; Hence $Y = 0$
- For $t > t_6$; $A = 0$, $B = 1$; Hence $Y = 0$



Based on the above, the output waveform for AND gate can be drawn as given (see figure).

S13. From the above figure, it follows that for the inputs A and B, the output of the AND gates is y'. Further, for the OR gate, the inputs are A and y' and the output is y. We know that output of AND gate is 1, when both the inputs are 1 and the output of OR gate is 1, when either of the two inputs is 1. Keeping these facts in view, the input-output combinations of the given circuit will be as given in table below.

A	B	y'	y
0	0	0	0
1	0	0	1
0	1	0	0
1	1	1	1

IInd Method: Now, $y' = A \,.\, B$

$\therefore$ $y = A + y'$

$= A + A \,.\, B = A \,.\, (1 + B)$

$= A \,.\, 1$

$= A$ $(\because\ 1 + B = 1)$

It follows that when $A = 0$, $B = 0$, then $y = 0$,

when $A = 1$, $B = 0$, then $y = 1$,

when $A = 0$, $B = 1$, then $y = 0$,

when $A = 1$, $B = 1$, then $y = 1$.

It follows that the above table (read columns A, B and y only) is the truth table for the given logic circuit.

S14. (a) ***Working of LED:*** LED is a forward biased p-n junction which converts electrical energy into optical energy of infrared and visible light region.

Being in forward bias, thin depletion layer and low potential barrier facilitate diffusion of electron and hole through the junction when high energy electron of conduction band combines with the low energy holes in valence band, then energy is released in the form of photon, may be seen in the form of light.

(b) Semiconductors with appropriate band gap (Eg) close to 1.5 eV are preferred to make LED size GaAs, CdTe etc.

The other reasons to select these materials are high optical absorption, availability of raw material and low cost.

(c) ***Use of LEDs:*** (i) LED can operate at very low voltage and consumes less power in comparison to incandescent lamps.

(ii) Unlike the lamps, they take very less operational time and have long life.

S15. The logic gate marked X is ***NAND gate***, while the gate marked as *Y* is ***OR gate***.

From the above figure, it follows that for the inputs *A* and *B*, the output of the NAND gate is y'. Further, for the OR gate, the inputs are *A* and y' and the output is *y*. We know that output of NAND gate is 0, only when both the inputs are 1 and the output of OR gate is 1, When either or both the inputs are 1. Keeping these facts in view, the input-output combinations for the given circuit will be as given in table below.

A	B	y'	y
0	0	1	1
1	1	0	1

IInd Method: Now, $y' = \overline{A.B}$

$\therefore$ $y = A + \overline{A.B}$

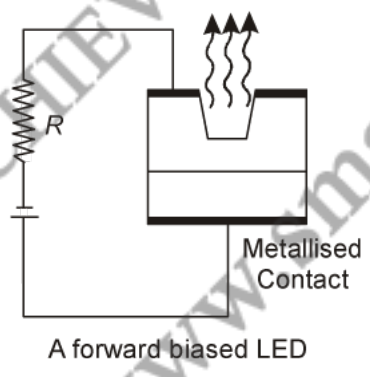
Applying De Morgan's second theorem, we get

$$y = A + \overline{A} + \overline{B} = 1 + \overline{B} = 1.$$

It follows that *y* will be 1, for both the input combinations and hence, in the above table (read columns *A*, *B* and *y* only) is the truth table for the given logic circuit.

S16. (a) Wavelength of light is controlled by band gap (E_g) of semiconductor material.

(b) Intensity of light emitted by the diode depends on concentration of impurity in junction diode.



S17. From the above figure, it follows that for the inputs *A* and *B*, the output of the OR gate is y'. Further, for the AND gate, the inputs are *A* and y' and the output is *y*. We know that the output of OR gates is 1, when either of the two inputs is 1 and output of AND gate is 1, when both the inputs are 1. Keeping these facts in view, the input-output combinations for the given circuit will be as given in table below.

A	B	y'	y
0	0	0	0
1	0	1	1
0	1	1	0
1	1	1	1

Aliter: Now, $y' = A + B$

$$y = A \cdot y'$$

$$= A \cdot (A + B) = A \cdot A + A \cdot B$$

$$= A + A \cdot B \qquad (\because\ A \cdot A = A)$$

$$= A$$

It follows that

when $A = 0$, $B = 0$, then $y = 0$,
when $A = 1$, $B = 0$, then $y = 1$,
when $A = 0$, $B = 1$, then $y = 0$,
when $A = 1$, $B = 1$, then $y = 1$.

It follows that in the above table (read columns A, B and y only) is the truth table for the given logic circuit.

S18. Truth table of given circuit is given below.

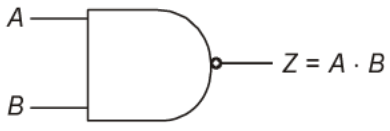
A	B	$X = \overline{A}$	$Y = \overline{B}$	$Z = \overline{X} + \overline{Y}$
0	0	1	1	0
1	0	0	1	0
0	1	1	0	0
1	1	0	0	1

This circuit is carries out by the logic operation of AND gate which can also be verified by De-Morgan's theorem.

$$Z = \overline{X + Y} = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} = A \cdot B$$

So, the circuit corresponds to AND gate.

Symbol



S19. The logic gate marked as X is NAND gate is y' and for the input y', the output of NOT gate is y. We know that output of NAND gate is 0, only when both the inputs are 1 and the not gate always inverts the input. Keeping these facts in view, the input-output combinations for the given circuit will be as given in the table below

A	B	y'	y
1	1	0	1
0	0	1	0

Aliter: Now, $y' = \overline{A \,.\, B}$

$\therefore$ $y = \overline{y'} = \overline{(\overline{A \,.\, B})}$

or $y = A \,.\, B$

Therefore, the given logic circuit functions as ***AND gate***.

It follows that

when $A = 1, \quad B = 1, \quad$ then $y = 1,$

when $A = 0, \quad B = 0, \quad$ then $y = 0,$

It follows that in the above table (read columns A, B and y only) is the truth table for the given logic circuit.

S20. $$Y = \overline{A} + \overline{B} = A \cdot B$$

Truth table of given circuit is given below.

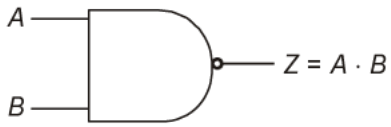
A	B	$X = \overline{A}$	$Y = \overline{B}$	$Z = \overline{X} + \overline{Y}$
0	0	1	1	0
1	0	0	1	0
0	1	1	0	0
1	1	0	0	1

This circuit is carries out by the logic operation of AND gate which can also be verified by De-Morgan's theorem.

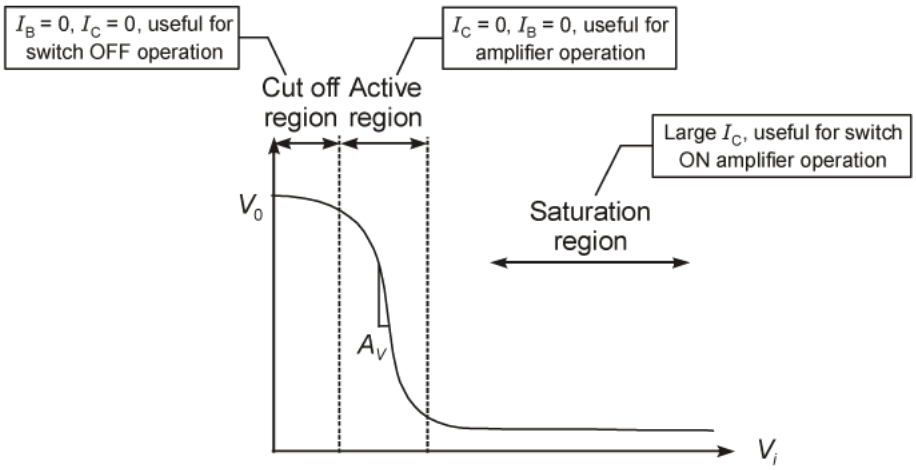
$$Z = \overline{X + Y} = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} = A \cdot B$$

So, the circuit corresponds to AND gate.

Symbol



S21.



Transfer characteristic of base-biased transistor

The active region of transfer characteristic curve operates as an amplifier.

(a) The input resistance, r_i of transistor in CE configuration is defined as the ratio of small change in base-emitter voltage to the corresponding small change in the corresponding small change in the base current, when the collector emitter voltage is kept constant *i.e.*,

$$r_i = \left(\frac{\Delta V_{EB}}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

(b) ***Output resistance:*** The ratio of variation of collector emitter voltage (V_{CE}) and corresponding change in collector current (ΔI_C) when base current remains constant, is called output characteristic curve.

$$\therefore \quad R_{\text{output}} = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B = \text{constant}}$$

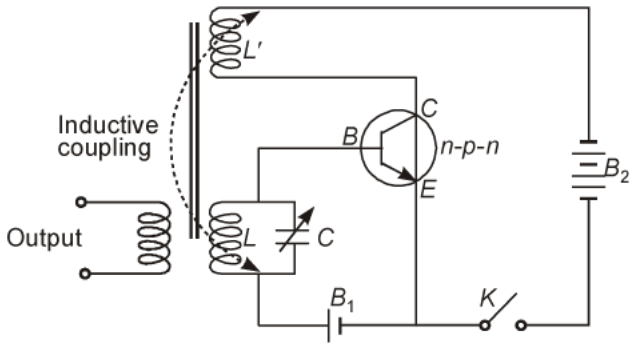
(c) The current amplification factor of a transistor in CE configuration is equal to the ratio of the small change in the collector current (ΔI_C) to the small change in base current when collector-emitter voltage is kept constant *i.e.*,

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

S22. ***Transistor amplifier as an oscillator:*** The main component of circuit are as follows:

(a) ***Tank circuit:*** An *L*-*C* parallel combination, in which damped energy oscillation take place between the *L*-*C* parallel combination whose frequency is given by

$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

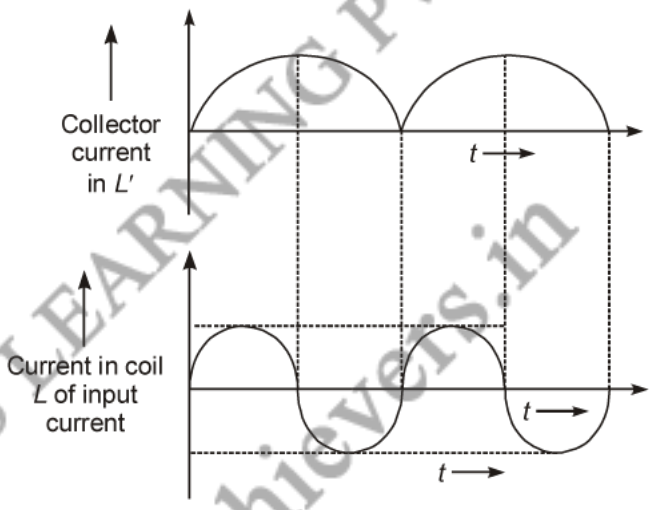


(b) ***Transistor amplifier:*** *n*-*p*-*n* transistor is used as CE amplifier.

(c) ***Feedback network:*** The phenomenon of mutual inductance is used to take a part of output, *L′* back into coil, *L*.

When the switch K is closed collector current begin to flow through, *L′*, which in turn increases the magnetic flux linked with *L′* and hence with *L*. This leads to produce an induce e.m.f. in *L*, which increases the forward bias. This also increases the base current and hence collector current along with the charging of capacitor takes place with upper plate as positive. This phenomenon is replaced again and again till the collector current reaches to its maximum value.

At maximum value of I_C, current through *L′* does not change and therefore, flux remain unchanged and e.m.f. *L′* and *L* reduces to zero. Now, the discharging of capacitor begins through *L*. The positivity of upper plate decreases and forward bias decrease which results in the form of decrease in base current and hence decrease in collector current. Thus phenomenon repeats till collector current reduces to zero and e.m.f. in the coil *L* also reduces to zero.



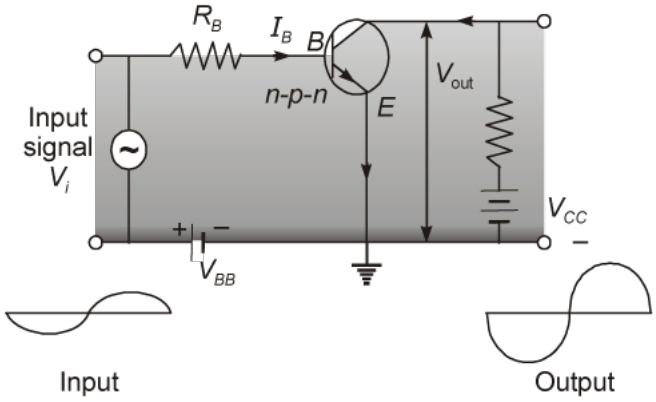
Thus, the time duration in which collector current grows from zero to maximum, the current in coil L of tank circuit complete its half cycle. The duration in which collector current reduces from maximum to zero, the current in *L′* completes, its half cycle.

The frequency of oscillation of energy is given by

$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

Thus, the *AC* of desired frequency and amplitude can be obtained by taking appropriate value of inductance, capacitance and strength of battery, *B*.

S23. (a) Circuit diagram of a common emitter amplifier



Voltage gain: It is equal to the ratio of small change in output voltage at the collector to that of change in input voltage *i.e.*,

$$A_V = \frac{\text{Output voltage}}{\text{Input voltage}} = \frac{\Delta V_{CE}}{\Delta V_{EB}} = \frac{(\Delta I_C)R_{out}}{\Delta I_B R_{in}} = \beta_{AC} \times \frac{R_{out}}{R_{in}}$$

$\Rightarrow$ Voltage gain = $\beta_{AC} \times$ Resistance gain

where, β_{AC} is AC current gain.

The active region of a transfer characteristic curve can be used to explain the transistor as an amplifier. The resistance of output circuit is large being in reverse bias and resistance of input circuit is low being in forward bias. When input voltage, V_{BE} comes in active region, I_C flows in output and V_0 varies significantly as

$$V_0 - V_{CE} = V_{CC} - I_C R_L$$

This change in output voltage is obtained as amplified form.

(b) NAND gates are terms as universal gates because all three basic gates namely AND, OR and NOT can be made, using NAND gate.

The given circuit perform the logic operations of AND gate as

$$Y = (A \,.\, B) = A \,.\, B$$